Advances in Atom and Single Molecule Machines
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Nanopackaging: From Nanomaterials to the Atomic Scale

Proceedings of the 1st International Workshop on Nanopackaging, Grenoble 27–28 June 2013

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Preface

Single atom and molecule manipulations are now possible thanks to the scanning tunneling microscope (STM) and its derivatives opening a new technological field, named "Atom Technology" with the objective to produce one-day atomic scale logic circuits. STM operates in ultra-high vacuum (UHV) and thanks to its picometer scale precision, is able to construct or pattern an atomic scale circuit on a specific surface. The electronic chip such achieved and connected will be only suitable for in situ operation in the UHV. The requirement for future applications is to get a standalone chip, similar to electronics ones currently produced. Consequently, it clearly appears a special need for developing a dedicated packaging technology for this new kind of chip. The most constraining specification concerns the UHV control inside the package. Moreover, the surface quality needs to as perfect as possible (atomic roughness and large terraces) with a controlled surface structure and material band gap suitable for atom by atom manipulations. Among the available existing materials, silicon (100) wafers, commonly used in microelectronics manufacturing, are very promising because they are satisfying the requirement of surface quality and benefit from the very important know-how developed in the microelectronics industry.

The first exploration of such a nano-packaging technology has been launched with the Integrated European Project AtMol on January 1, 2011. A first international AtMol workshop took place at MINATEC, France, on June 2013 with participants coming from university laboratories, research institutes, and industries. This volume compiles most of the contributions presented during this event.

Besides the first driver for nano-packaging as described above, this workshop was also opened to a second trend which concerns nanomaterials for microelectronics. Nanomaterials bring new solutions for detection not only in sensor application or in passive components technology, but also in improving packaging of actual microelectronics components. In particular, CNT could be a solution for highly electrically and thermally conductive interconnections. CNT incorporated in an insulator matrix could also make the composite conductor. Biomaterials also appear as a new solution for nanoscale interconnections. By analyzing actual and future microelectronics and packaging requirements, it seems that solutions could

be found at the interface between a top-down approach lying on silicon and atomic scale technologies and a bottom-up approach consisting in the integration of functionalized nano-objects.

We thank the European Commission's ICT-FET program and the staff of Springer Verlag for their help in producing this book. The organizing committee also wishes to thank all the participants for their fantastic participation to the workshop.

Xavier Baillin
Christian Joachim
Gilles Poupon

Contents

Utilization of Peridynamic Theory for Modeling at the Nano-Scale

E. Oterkus, C. Diyaroglu, N. Zhu, S. Oterkus and E. Madenci

Abstract Peridynamic theory is a new continuum mechanics formulation that has several advantages over the traditional approaches, such as Classical Continuum Mechanics (CCM) and Molecular Dynamics (MD). Due to its length-scale parameter, horizon, it is capable of capturing phenomena occurring at different length scales, including the nano-scale. Furthermore, van der Waals forces can be represented in a straightforward manner using a buffer-layer approach. In this chapter, various demonstration problems are presented to show the capability of peridynamics at the nano-scale, including nano-indentation and failure analysis of graphene sheets.

1 Introduction

Traditionally, there exist two main approaches to simulate the mechanical behavior of materials at the nano-scale. The first approach is based on Classical Continuum Mechanics (CCM) when the continuum assumption is valid. When nano-scale effects become significant, it is no longer applicable since it does not have a length-scale parameter. Furthermore, its equation of motion is not suitable for problems including discontinuities since the spatial derivatives are not defined in such cases. The second approach is based on Molecular Dynamics (MD). It is a powerful tool as long as the interactions between atoms and molecules are well defined. However, even with current powerful supercomputers, the total simulation time and size of the models are still limited. Therefore, it is necessary to use a methodology that is based on continuum mechanics and have a length-scale

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parameter to capture the nano-scale effects. Furthermore, it should be applicable for problems with discontinuities. Such an approach was introduced by Silling [1]; it has been successfully used for modeling metallic and composite structures, nano-fiber networks, etc. An extensive literature survey is given in a recent book on peridynamics by Madenci and Oterkus [2].

This chapter presents a brief overview of peridynamics, and how it can be used at the nano-scale. Furthermore, it presents solutions to various examples to demonstrate its capability.

2 Peridynamic Theory

2.1 Peridynamic Formulation

Peridynamics is based on continuum assumptions in which the body is composed of infinitesimally small volumes called material points. As opposed to CCM, a material point can interact with material points in its nearest neighborhood and also with other material points inside an influence domain, $\Re$, called the horizon, as shown in Fig. 1.

The interaction (bond) between material points is defined through peridynamic forces, $\mathbf{f}$. Therefore, the equation of motion of a material point at $\mathbf{x}$ can be obtained by integrating all peridynamic forces acting on that material point,

$$\rho \frac{\partial^2 \mathbf{u}(\mathbf{x},t)}{\partial t^2} = \int_{\Re} \mathbf{f}(\mathbf{u}(\mathbf{x}',t) - \mathbf{u}(\mathbf{x},t), \mathbf{x}' - \mathbf{x}, t) dV_{\mathbf{x}'} + \mathbf{b}(\mathbf{x},t) \tag{1}$$

in which $\mathbf{u}$ is the displacement vector field, $\mathbf{b}$ is a prescribed body-force density field, t is time, ρ is mass density in the reference configuration, and $\mathbf{x}'$ is the material point interacting with material point $\mathbf{x}$, as shown in Fig. 1. According to the original definition of peridynamics, i.e., bond-based formulation, the peridynamic force, $\mathbf{f}$,

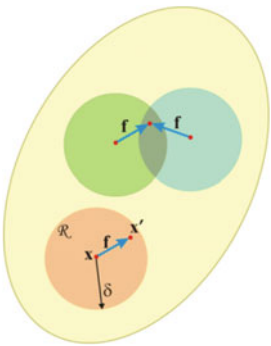

Fig. 1 Interaction of a material point with its neighboring points

can be assumed as equal in magnitude and opposite to the direction of the vector between two interacting material points in the deformed configuration.

The form of the peridynamic force should be chosen based on the characteristic of the material. For instance, the strain-hardening behavior in peridynamic theory can be achieved by defining each peridynamic bond as an elastic perfectly plastic material [3]. Because all bonds do not yield at the same time, the overall behavior of the structure exhibits strain hardening. The force–stretch relation shown in Fig. 2 can be expressed as

$$f = \begin{cases} cs_Y, & \text{if } s > (s^* + s_Y) \\ c(s - s^*), & \text{if } s > (s^* - s_Y) \\ -cs_Y, & \text{if } s < (s^* - s_Y) \end{cases} \tag{2}$$

where c is the peridynamic constant, which can be defined in terms of Young's modulus, E, of CCM as

$$c = \frac{12E}{\pi\delta^4} \tag{3}$$

and s is the stretch between two material points $\mathbf{x}$ and $\mathbf{x}'$, which can be defined as

$$s = \frac{|(\mathbf{x}' + \mathbf{u}') - (\mathbf{x} + \mathbf{u})| - |\mathbf{x} + \mathbf{u}|}{|\mathbf{x} + \mathbf{u}|}. \tag{4}$$

In Eq. (2), s_Y represents the bond yield stretch and s^* represents the permanent bond stretch as a result of loading and unloading. Non-brittle material points certainly exhibit plastic deformation when they experience a stress state near the ultimate strength of the material. Therefore, the value of the bond yield stretch can be obtained using the ultimate strength value of the material.

If the total stress value at a material point $\mathbf{x}$ is computed (see Fig. 3) and equated to the ultimate strength value of the material,

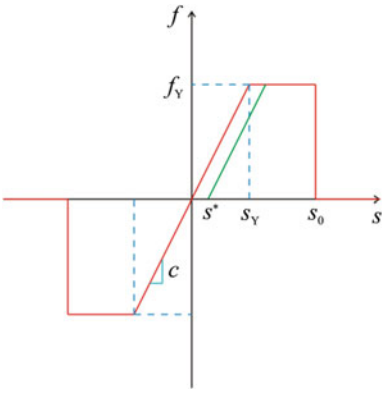

Fig. 2 Force-stretch relation for an elastic-perfectly plastic peridynamic bond

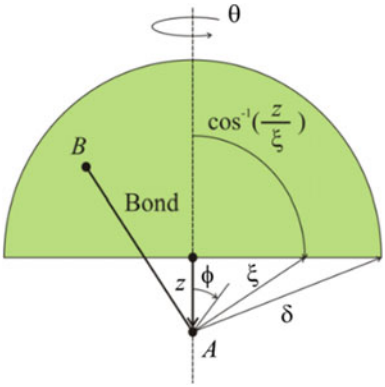

Fig. 3 Domain used for the stress computation in PD theory

$$\sigma_{\text{ult}} \approx \int_0^{\delta} \int_0^{2\pi} \int_z^{\delta} \int_0^{\cos^{-1}(z/\xi)} f_Y \, \xi^2 \cos(\phi) \sin(\phi) d\phi \, d\xi \, d\theta \, dz = \frac{\pi f_Y \delta^4}{6}, \tag{5}$$

and using the bond force-stretch relation shown in Fig. 2,

$$f_Y = c s_Y \tag{6}$$

leads to the bond yield stretch value in terms of the ultimate strength as

$$s_Y = \frac{\sigma_{\text{ult}}}{2E}. \tag{7}$$

Failure introduction in a peridynamic formulation is a straightforward process. In the solution phase, distances between material points are monitored and bond stretch is computed. When the stretch between two points exceeds the critical (failure) stretch, s_0, value (see Fig. 2), the interaction between these material points is terminated. Termination of the interaction between material points can be associated with the failure of the material by modifying the peridynamic force relation given in Eq. (2) by introducing the failure parameter $\mu(\mathbf{x}' - \mathbf{x}, t)$,

$$f = \begin{cases} \mu(\mathbf{x}' - \mathbf{x}, t) c s_Y, & \text{if } s > (s^* + s_Y) \\ \mu(\mathbf{x}' - \mathbf{x}, t) c (s - s^*), & \text{if } s > (s^* - s_Y) \\ -\mu(\mathbf{x}' - \mathbf{x}, t) c s_Y, & \text{if } s < (s^* - s_Y) \end{cases} \tag{8}$$

where the failure parameter can be defined as

$$\mu(\mathbf{x}' - \mathbf{x}, t) = \begin{cases} 1 & \text{if } s(\mathbf{x}' - \mathbf{x}, t') < s_0 \text{ for all } 0 < t' < t \\ 0 & \text{otherwise} \end{cases} \tag{9}$$

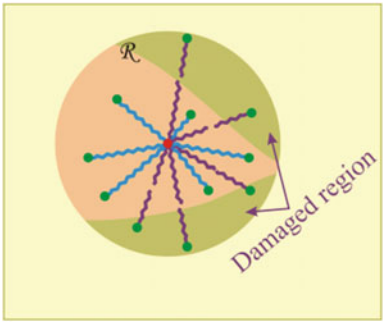

Fig. 4 Damaged and undamaged regions for a point

Damage is treated as part of the constitutive model through irreversible breakage of interactions, as depicted in Fig. 4.

The broken interactions may align themselves along surfaces that form cracks, and the deformation is discontinuous across such a crack, yet the governing equations of peridynamic theory remain valid. The local damage at material point $\mathbf{x}$, $\varphi(\mathbf{x}, t)$, is the ratio of the amount of broken interactions to the total amount of interactions and can be expressed as

$$\varphi(\mathbf{x}, t) = 1 - \frac{\int_{\Re} \mu(\mathbf{x}' - \mathbf{x}, t) dV_{\mathbf{x}'}}{\int_{\Re} dV_{\mathbf{x}'}}. \tag{10}$$

Thus, the damage in materials is simulated in a much more realistic manner compared to other continuum-based methods, without resorting to complicated special algorithms. The formulation is capable of modeling an arbitrary number of dissimilar materials in a structure. Another important feature of the peridynamic theory is its treatment of material interfaces. Alternate bond force/stretch relationships can be specified for the interactions between dissimilar materials.

2.2 *Numerical Solution*

The equation of motion given in Eq. (1) is difficult to solve analytically. Instead, the solution can be obtained numerically. The problem domain can be discretized into small volumes and each volume can be represented by a (collocation) point located at the center of the volume, as shown in Fig. 5. Each point in the body can interact with other points inside its domain of influence (horizon) using peridynamic bonds (forces) between them, as demonstrated in Fig. 6. For instance, point k interacts with six other points, j, inside its horizon and these are $j = k - 1$, $k - 2$, $k - 3$ $k + 1$, $k + 2$, $k + 3$. Therefore, the peridynamic equation of motion at point k can be expressed in a discrete form as

$$\rho\ddot{u}_{(k)} = \sum_{j=1}^{N} f_{(k)(j)} V_{(j)} + b_{(k)}, \tag{11}$$

where $f_{(k)(j)}$ is the peridynamic force between points k and j, $V_{(j)}$ is the volume of point j, and N is the number of points inside the horizon of point k.

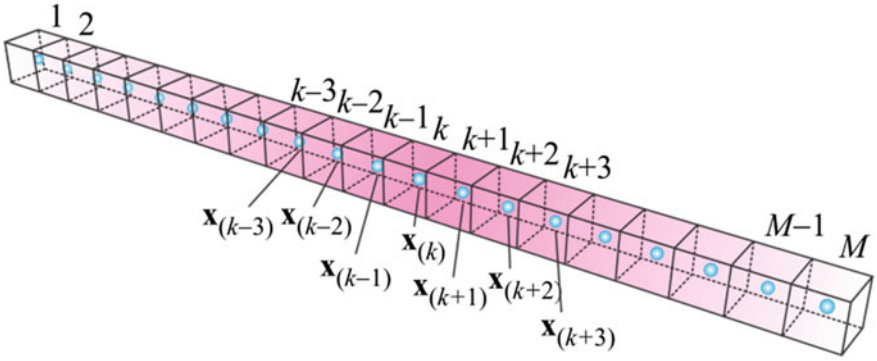

Fig. 5 Discretization and (collocation) points in a body

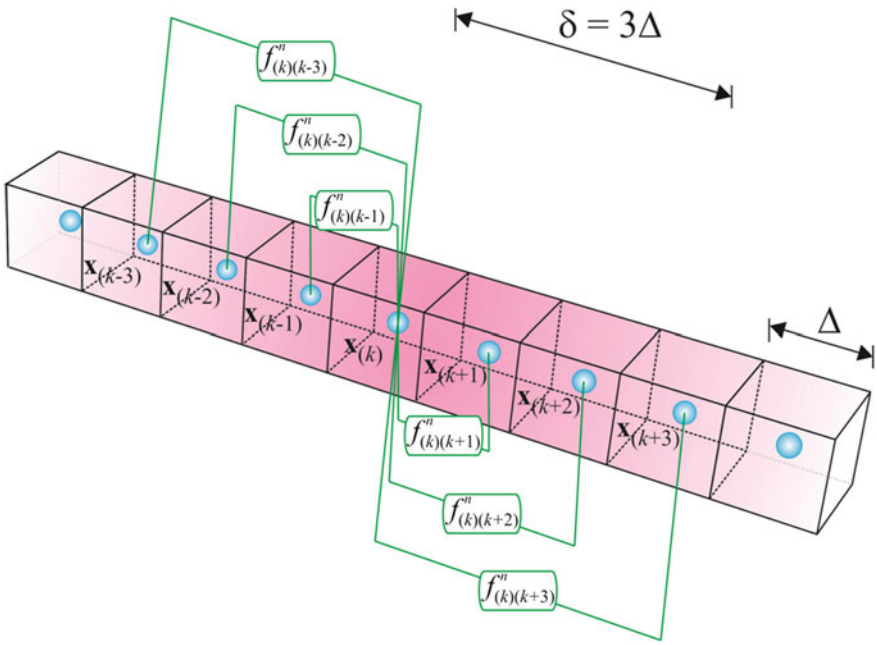

Fig. 6 Interaction of material points within the horizon

2.3 Definition of Contact in Peridynamics

The contact phenomenon can be defined in peridynamics using a simple algorithm if one of the bodies in contact can be assumed as a rigid body. If there is a physically unacceptable interpenetration between the two bodies, the material points of the deformable body that are inside the rigid body are moved to the surface of the rigid body, developing a contact surface between the two bodies.

Therefore, the modified velocity vector of the material point $\mathbf{x}$ for the next time increment, $\bar{\mathbf{v}}^{t+\Delta t}$, can be computed as

$$\bar{\mathbf{v}}^{t+\Delta t} = \frac{\bar{\mathbf{u}}^{t+\Delta t} - \mathbf{u}^{t}}{\Delta t}, \tag{12}$$

where $\bar{\mathbf{u}}^{t+\Delta t}$ is the modified displacement vector at time $t + \Delta t$, $\mathbf{u}^{t}$ represents the displacement vector at time t, and Δt is the time increment value. The contribution of the material point i to the reaction force from the deformable body to the rigid body at time $t + \Delta t$, $\mathbf{F}_i^{t+\Delta t}$, can be found as

$$\mathbf{F}_i^{t+\Delta t} = -1 \times \rho_i \frac{\left(\bar{\mathbf{v}}_i^{t+\Delta t} - \mathbf{v}_i^{t+\Delta t}\right)}{\Delta t} V_i, \tag{13}$$

where $\mathbf{v}_i^{t+\Delta t}$ is the velocity vector at time $t + \Delta t$ before relocating the material point i, and ρ_i and V_i are the density and volume of the material point i, respectively. Summation of the contributions of all material points inside the rigid body leads to the total reaction force on the rigid body at time $t + \Delta t$, $\mathbf{F}^{t+\Delta t}$,

$$\mathbf{F}^{t+\Delta t} = \sum_{i=1}^{M} \mathbf{F}_i^{t+\Delta t} \lambda_i^{t+\Delta t}, \tag{14}$$

where

$$\lambda_i^{t+\Delta t} = \begin{cases} 1 & \text{if the point } i \text{ is inside the rigid body} \\ 0 & \text{if the point } i \text{ is outside the rigid body} \end{cases} \tag{15}$$

and M indicates the total number of material points in the rigid body.

2.4 Peridynamic Formulation at Nano-Scale: Buffer Zone Approach

The effect of van der Waals forces that exist at the nano-scale is included in the peridynamic formulation based on the concept of a buffer zone. A soft buffer material is represented using two different peridynamic bonds, i.e., a normal bond and a diagonal bond, as shown in Fig. 7.

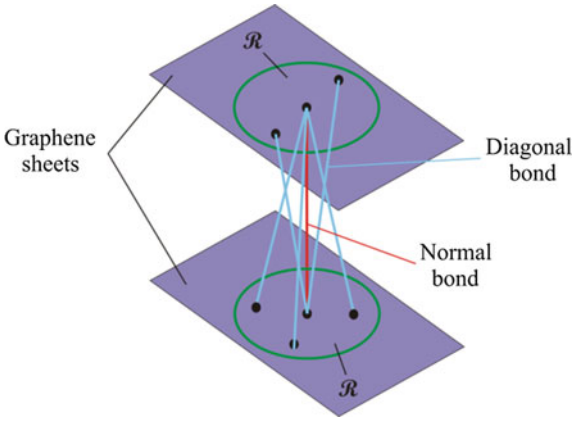

Fig. 7 Normal and diagonal bonds representing buffer material between graphene sheets

Their bond constants, c_n and c_d, respectively, can be expressed as

$$c_d = \frac{E_{\text{buffer}}}{h\bar{V}} \tag{16a}$$

and

$$c_d = \frac{2G_{\text{buffer}}}{\pi h} \frac{1}{\left(\delta^2 + h^2 \ln\left(\frac{h^2}{\delta^2+h^2}\right)\right)}, \tag{16b}$$

where E_{buffer} and G_{buffer} are Young's and shear moduli, respectively, and $\bar{V}$ is the volume of a material point. The normal bond relates the bond force to the stretch as

$$f(\mathbf{u}' - \mathbf{u}, \mathbf{x}' - \mathbf{x}, t) = c_n s. \tag{17}$$

The diagonal bond relates the bond force to the change in angle of the bond from its original configuration, φ,

$$f(\mathbf{u}' - \mathbf{u}, \mathbf{x}' - \mathbf{x}, t) = c_d \, \varphi \, \Delta^2, \tag{18}$$

where Δ is the edge length of the sub-domain (grid size).

3 Wave Dispersion in Peridynamics

The CCM does not have a length-scale parameter. Therefore, it is incapable of capturing phenomena occurring at lower scales that can affect the macro-scale behavior. On the other hand, the horizon parameter in peridynamics, which defines the domain of influence of peridynamic interactions, serves as a length-scale

parameter. In order to see the effect of horizon at lower scales, it is beneficial to investigate the wave dispersion phenomenon [1, 4–6].

In order to analyze the wave dispersion characteristics of peridynamics, a one-dimensional bar with a constant cross-sectional area, A, is considered. For this simple structure, the peridynamic equation of motion can be reduced to

$$\rho\,\ddot{u} = \int_{-\delta}^{\delta} \frac{c(u' - u)}{|x' - x|} A d\xi. \tag{19}$$

Substituting the wave solution, $u(x,t) = u_0\, e^{i(kx-\omega t)}$, into Eq. (19) results in

$$\rho\omega_{\mathrm{pd}}^2 = 2\int_0^{\delta} \frac{c}{\xi}(1 - \cos(k\xi))A d\xi, \tag{20}$$

in which k is the wave number and ω_{pd} is the peridynamic angular wave frequency.

Solution of Eq. (20) yields the dispersion relationship of the peridynamic formulation for a one-dimensional bar. Furthermore, as indicated by Silling [1], in the limit of long-wave lengths (small k), the integral in Eq. (20) can be simplified by taking into account only the first three terms of the Taylor series expansion for cosine function

$$\cos(k\xi) = 1 - \frac{(k\xi)^2}{2!} + \frac{(k\xi)^4}{4!}. \tag{21}$$

Substituting Eq. (21) into Eq. (20) and performing integration lead to

$$\omega_{\mathrm{pd}}^2 = \frac{E}{\rho}\left(k^2 - \frac{\delta^2 k^4}{24}\right). \tag{22}$$

Furthermore, as the horizon size approaches zero, i.e., $\delta \to 0$, the peridynamic theory should converge to CCM as a special case. Therefore, Eq. (22) recovers the dispersion relationship of CCM:

$$\omega_{\mathrm{pd}} = \omega_{\mathrm{ccm}} = \pm\sqrt{\frac{E}{\rho}}k. \tag{23}$$

In order to compare the dispersion characteristics of peridynamics and CCM, the following properties of the bar are considered: Young's modulus, $E = 200\,\mathrm{GPa}$, horizon size, $\delta = 10^{-8}$ m, and density, $\rho = 8000\,\mathrm{kg/m^3}$.

Figure 8 demonstrates the wave frequency variation with the wave number (wave length) from both CCM and PD formulations. In the case of a long-wave limit, i.e., k is small, both approaches behave similarly. However, as the wave number increases, the PD wave frequency diverges from that of CCM. In other

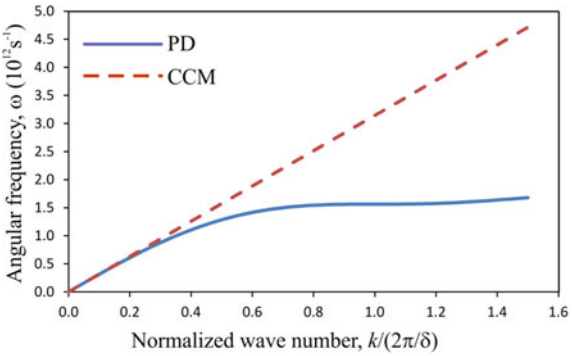

Fig. 8 Comparison of angular frequency variation with wave numbers from PD and CCM approaches

words, peridynamics is capable of representing a dispersive medium, which is widely seen in real materials and structures. This comparison clearly indicates one of the superior characteristics of PD theory with respect to CCM.

4 Demonstration Problems

4.1 Nano-Indentation

In the first demonstration case, the problem of nano-indentation of silicon nitride is considered based on a MD study by Walsh et al. [7]. The in-plane dimensions of the 30–nm-thick film are specified as 60.6 nm. The rigid pyramid indenter with a square base is moved with a velocity of $v_0 = 100$ m/s. During the indentation process, a force–displacement relation is obtained for both loading and unloading conditions. The peridynamic model is generated by 108,000 material points as opposed to 10 million atoms of MDS. The model parameters used in the peridynamic simulation are: bond constant $c = 18.49\,\text{nN} \cdot \text{nm}^{-6}$, yield stretch $s_Y = 0.05$, horizon radius $\delta = 3.015$ nm, and grid spacing $\Delta = 1$ nm. In the solution, no damage is allowed. As depicted in Fig. 9, there is a very good agreement between the force–indentation depth relations obtained from the two different approaches. Note that the peridynamic results can be achieved using significantly less computational time. Finally, Fig. 10 shows how the yielded portion of the material evolves during loading and unloading phases.

4.2 Single-Layer Graphene Failure

As a second demonstration case, a graphene layer with an initial edge notch subjected to tensile loading is considered. This problem was originally considered by

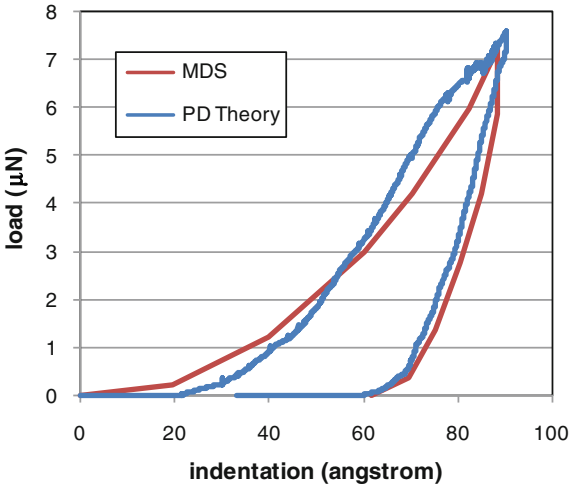

Fig. 9 Force-displacement curve obtained by using (*red*) molecular dynamics (Walsh et al. [7]) and (*blue*) peridynamic theory

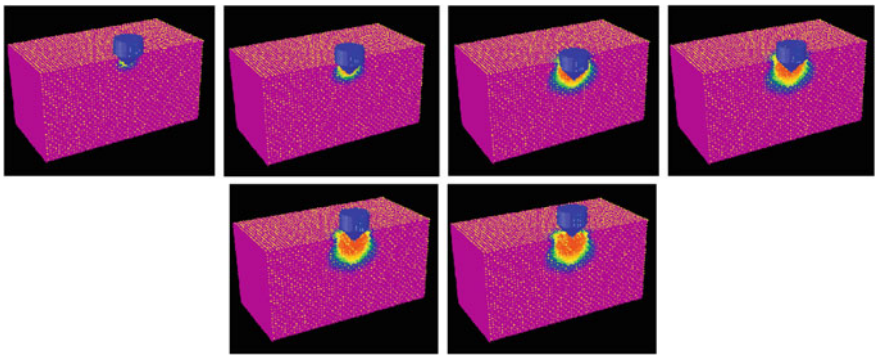

Fig. 10 Evolution of the yielded portion of the structure as time progresses during loading and unloading

Omeltchenko et al. [8], using MDS with 2 million particles. In this problem, two single graphene layers with different molecular orientations with respect to the loading direction, G(1, 1) (armchair) and G(1, 0) (zigzag), are considered, as illustrated in Fig. 11. Graphene layers have vertical and horizontal sides of 200 nm and 150 nm, respectively. In both cases, a constant strain of 12 % was applied in the horizontal direction, and an initial notch of 3 nm was placed at the center of the bottom boundary. The MDS of the G(1, 1) graphene layer yielded a self-similar propagation of the crack, as shown in Fig. 12a. However, the G(1, 0) simulations show that the crack immediately branches into two, which subsequently leads to

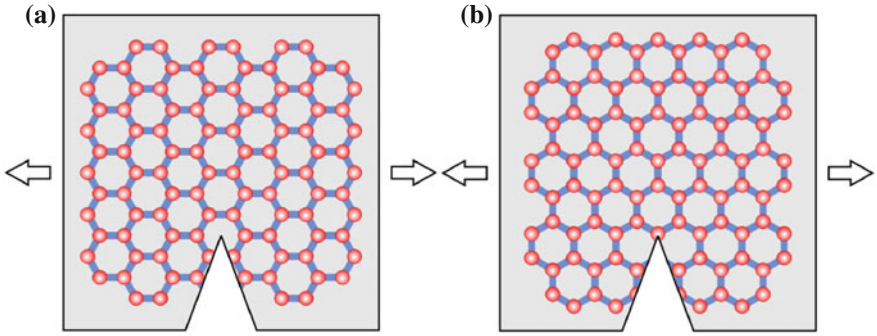

Fig. 11 Orientation of graphene layers with respect to loading direction: **a** armchair G(1-1), **b** zigzag G(1-0)

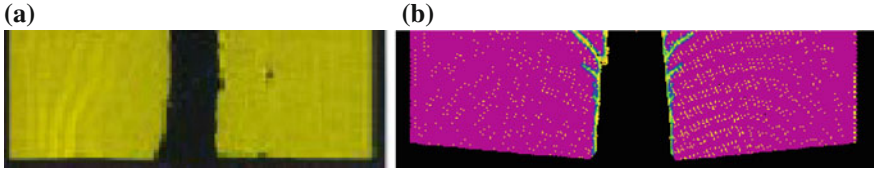

Fig. 12 Comparison of crack patterns for graphene with armchair G(1-1) orientation: **a** MDS, **b** peridynamic theory

multiple sub-branches of their own (Fig. 13a). The dynamic nature of crack propagation is evident in this case as some of the smaller branches stop propagating when growth becomes energetically inefficient (due to the larger branch growth). Also reported in their study is that the fracture toughness of the armchair layer is larger than that of the zigzag layer.

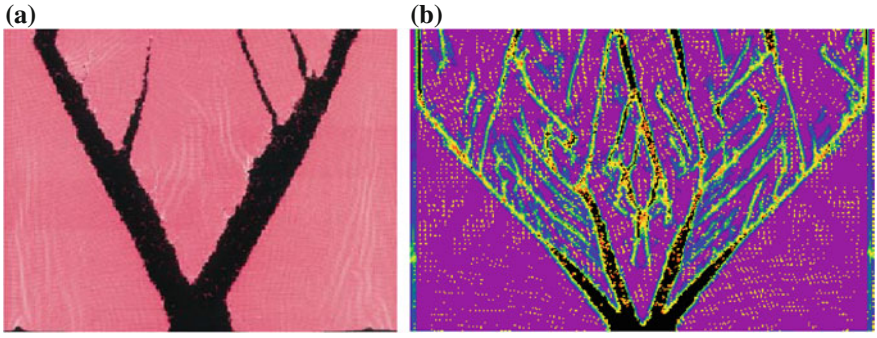

Fig. 13 Comparison of crack patterns for graphene with zigzag G(1-0) orientation: **a** MDS, **b** peridynamic theory

Both of these cases are also solved using the peridynamic theory. Young's modulus is specified as $E = 1\,\text{TPa}$, which is the commonly accepted value in the literature. The domain is discretized with a regular grid using 120,000 material points, which is 16 times less compared to the number of MDS particles used by Omeltchenko et al. [8]. Corresponding grid size and horizon size are 0.5 nm and 1.5075 nm, respectively. It is worth noting that the two peridynamic models (i.e., one for the armchair and the other for the zigzag) are identical in all aspects except for the critical stretch value, s_0. Silling and Askari [9] demonstrated that the critical stretch value increases with increasing critical energy release rate, which implies a similar relationship with fracture toughness (i.e., increased fracture toughness means larger critical stretch). In this study, critical stretch values for the armchair and zigzag configurations are assumed as 0.25 and 0.1, respectively.

The peridynamic failure patterns for the armchair (G(1, 1)) and zigzag (G(1, 0)) graphene layers are depicted in Figs. 12b and 13b, respectively. The armchair simulation (Fig. 12b) exhibits a self-similar growth, as was observed in MDS. Moreover, the peridynamic simulation of zigzag graphene layer (Fig. 13b) produces a complex branching behavior of the crack, as in the MDS study. Even though the number of main branches differs, the behaviors of the branches (and the sub-branches) exhibit remarkably similar trends. In both MDS and peridynamic simulations, some of the sub-branches stop growing due to the growth of the main branches.

4.3 Multi-Layer Graphene Failure

An analysis similar to the previous case is also performed for multi-layered graphene sheets in order to see the effect of molecular orientations in the sequence on the overall failure mode of the structure. The peridynamic model is obtained by including a buffer material layer between graphene sheets to represent existing van der Waals forces. The geometrical, material, and peridynamic parameters for each graphene sheet are same as those in the previous case. For the buffer material, Young's and shear moduli are specified as 24.33 GPa and 9.12375 GPa, respectively, as suggested by Yang et al. [10]. The spacing between graphene sheets is specified as 0.34 nm, which also corresponds to the thickness of the buffer layer in which failure is not allowed.

Four different stacking sequences for three-layer graphene sheets are considered. For the commensurate case having all armchair-type graphene layers, one observes a failure mode similar to the single-layer case (Fig. 14a–c). However, if a zigzag-type graphene sheet is placed between two armchair-type graphene sheets, although a self-similar type of failure mode continues to exist for the armchair-type graphene sheets, a sharp crack tip is observed, as opposed to the blunt crack tip in the commensurate case (Fig. 15a, c). For the zigzag-type graphene layer at the center, a self-similar crack growth with many sub-branches occurs, as opposed to the significant branching behavior in the single-layer case (Fig. 15b).

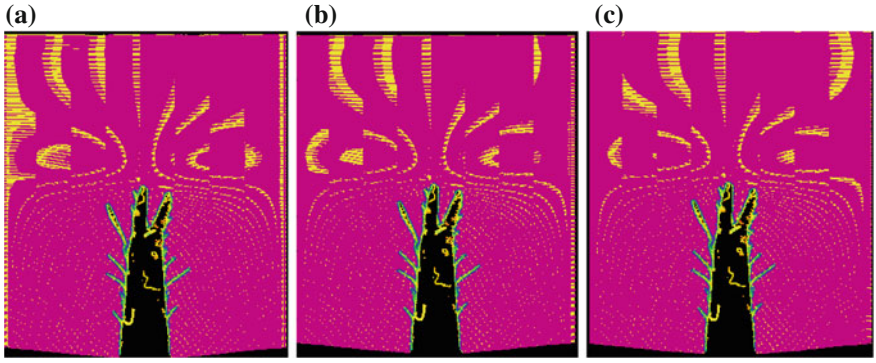

Fig. 14 Comparison of crack patterns for three-layer graphene sheets with all armchair G(1-1) orientations using peridynamic theory: **a** *bottom layer*, **b** *center layer*, **c** *top layer*

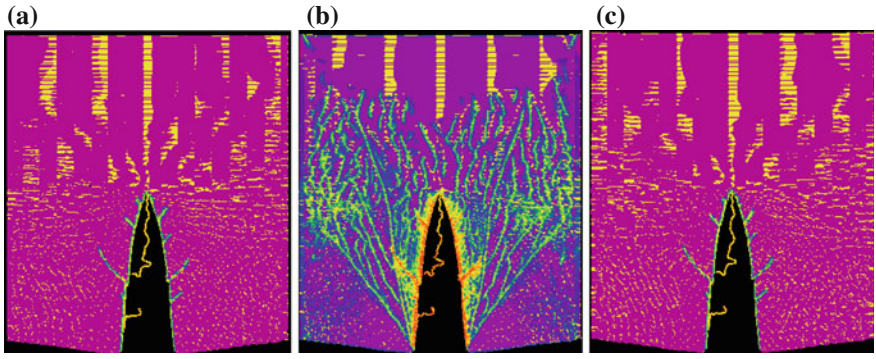

Fig. 15 Comparison of crack patterns for three-layer graphene sheets using peridynamic theory: **a** *bottom layer* with armchair G(1-1) orientation, **b** *center layer* with zigzag G(1-0) orientation, **c** *top layer* with armchair G(1-1) orientation

Similar to the commensurate case of armchair-type graphene sheets, the commensurate case of the zigzag-type of three-layer graphene sheets results in a failure pattern similar to the single-layer case (Fig. 16a–c). However, placing an armchair-type graphene sheet between two zigzag-type graphene sheets leads to a failure mode that is a combination of self-similar growth and branching (Fig. 17a–c).

Based on the results obtained for three-layer graphene sheets, it is clear that van der Waals forces are strong enough to influence the failure behavior of individual graphene sheets. From this point of view, graphene sheets behave more like a fiber-reinforced composite laminate, in which the failure modes are dependent on the stacking sequence of its constituents [11].

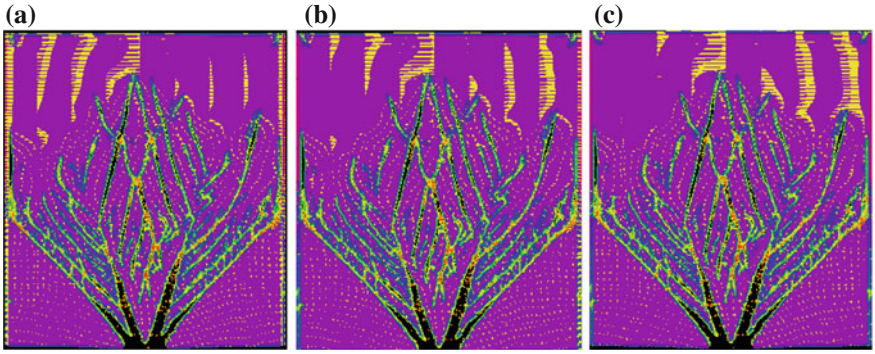

Fig. 16 Comparison of crack patterns for three-layer graphene sheets with all zigzag G(1-0) orientations using peridynamic theory: **a** *bottom layer*, **b** *center layer*, **c** *top layer*

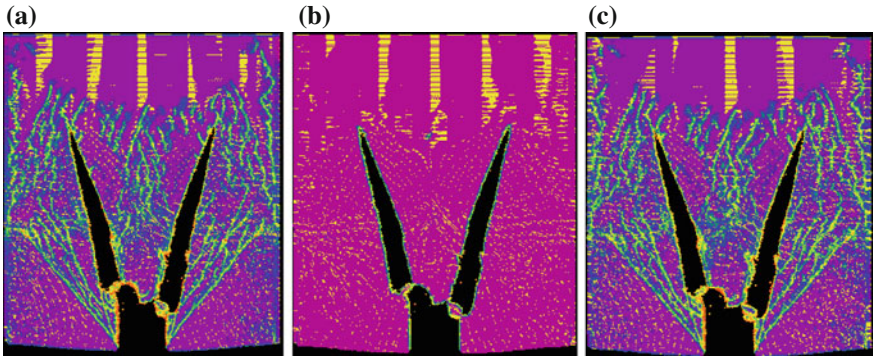

Fig. 17 Comparison of crack patterns for three-layer graphene sheets using peridynamic theory: **a** *bottom layer* with zigzag G(1-0) orientation, **b** *center layer* with armchair G(1-1) orientation, **c** *top layer* with zigzag G(1-0) orientation

5 Conclusions

Based on various demonstration problems considered in this chapter, it can be concluded that peridynamics is a powerful technique in capturing complex fracture modes including branching. Also, it is straightforward to define contact between bodies, and it can be used for nano-indentation analysis. Moreover, using a buffer-layer approach, it is demonstrated that the molecular orientations in the sequence of graphene sheets can have a significant effect on the overall failure of the material.

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DNA Metallization Processes and Nanoelectronics

Arianna Filoramo

Abstract DNA fascinates for its exceptional assembling properties which make it an ideal candidate to encode instructions for nano-scale assembly. However, to utilize DNA not only as a positioning scaffold but also for electrical interconnections, it is pragmatically envisioned to metallize it. Here, an overview of DNA metallization processes is presented.

1 Introduction

The Silicon-CMOS technology is the base of present hardware technology for information processing. Until now, its evolution is governed by Moore' laws (1970s), stating that microprocessor performance (defined as the number of transistors on a chip) doubles every 18 months. However, even if no doubt is raised for its future use and deployment, the International Technology Roadmap for Semiconductors (ITRS) [1] still predicts that the present CMOS technology will benefit by the contribution of complementary approach and emerging material and devices.

This motivates the research community to study and develop alternative nanofabrication technologies, which could possibly enable the production and manipulation of well-defined structures at the nanoscale level. Indeed, it is undeniable that conventional technologies based on "top-down" approaches are foreseen to experiment difficulties. At this scale, self-assembly, and more generally, "bottom-up" approaches appear to be a reasonable way to assemble nano-objects into circuits with a two-dimensional and/or three-dimensional layout. In particular, self-assembly is also identified as the one promising way to reduce significantly the fabrication costs compared to what is expected for standard top-down silicon-based

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devices. Indeed, the basic idea of self-assembly is to use a process involving the spontaneous self-ordering of substructures into superstructures. This spontaneous self-ordering is due to specific chemical or physical properties of matter, and relies on the natural tendency of the system to search for a stable configuration.

Among the new methodologies based on bottom-up approaches for future nanotechnology, the exploration of the bio-directed assembly for organizing nano-objects is one of the most promising ones. Indeed, the nanoscale is the natural scale on which biological systems build up their structural elements, and biological molecules have already shown great potential in the fabrication and construction of nanostructures and devices. In this context, the DNA molecule is of particular interest, as highlighted by the increasing number of recent works devoted to the study of its physical properties and implementation in nano-constructions and nano-electronics. Indeed, the DNA molecule has already been successfully used to build up nanostructures [2, 3] or scaffolds for nanoparticles' assembly [4–7]. Moreover, one can envision its use for the assembly of devices [8]. The key advantage in using DNA as a scaffold for these constructions is that its intra- and inter-molecular interactions are the most readily known, easily engineered, and reliably predicted. Note that in this approach the genetic value of DNA is completely disregarded; only its structure and self-assembly properties are considered. The information contained in DNA sequences can be envisioned to code: (i) the assembly of the scaffold, (ii) its selective attachment on the surface microscale electrodes, (iii) the positioning of nano-objects or nanodevices on the scaffold and (iv) the realization of electrical connections and circuitry.

Here, we do not mean to present an exhaustive review of DNA-directed assembly techniques, but rather a focused discussion onto DNA metallization.

2 Why Is It Necessary to Metallize DNA?

The transport properties of DNA molecules have recently generated heated debate among scientists, as evidence both for and against the hypothesis of DNA as a conducting wire has been piled up. While no full consensus is completely reached yet, the extensive transport measurements carried out on single DNA molecules and DNA bundles strongly suggest that DNA in the dry state deposited on a substrate is a good insulator [9–12] and thus not useful as a conducting element. We believe that in spite of its somehow negative sense, such a conclusive statement is of great importance in defining strategies for implementing a DNA-based technology. Indeed, it becomes now clear that to achieve an electrical connecting use of DNA strands, it is necessary to proceed to their metallization. During the past 10 years, we have seen the rise of numerous methods to metallize DNA scaffolds and we will summarize in the following the main aspects and results.

3 The DNA Metallization Process

The feasibility of this biotemplating approach was firstly shown by Braun et al. [13]. The authors first immobilized a dsDNA strand between two electrodes. Then, they treated it with silver ions in order to perform an Ag^+/Na^+ ion-exchange and replace the natural sodium counter ions of the dsDNA backbone with silver ones. Successively, these silver ions were subjected to a chemical reduction process by hydroquinone (reducing agent) to form small silver aggregates. Finally, the silver nanoclusters fixed on the dsDNA strand were autocatalytically grown (using an acidic solution of hydroquinone and silver ions) to give a granular (100-nm width) nanowire contacting the two electrodes.

The majority of dsDNA metallization processes follows the same principle and can be decoupled in terms of successive steps, as schematically shown in Fig. 1 and discussed below.

The first step consists in biomolecule activation: the metal ions or metal complexes bind to dsDNA (Fig. 1a). The activation can take place by ion exchange mechanism (such as discussed above for silver [13]) on the DNA backbone or by insertion of the metal complexes between the DNA bases (like platinum or palladium complexes [14]).

In the second step, the bound metal ions or metal complexes are usually treated with a reducing agent (Fig. 1b). This converts them in metal nanoclusters fixed on the DNA strand. The more used reducing agents are dimethylaminoborane [15, 16], hydroquinone [13], and sodium borohydride [17]. An interesting variant has been proposed by Keren et al. [18, 19], who fixed the reducing agent (glutaraldehyde) directly onto the dsDNA strand in order to enhance specificity and reduce parasitic unwanted background metallization.

The key point is that at the end of these two steps, the dsDNA strand has some small metal nanoclusters fixed on it (as represented in Fig. 1c), which will successively act as "seeds" for the metallization of the DNA molecules.

The third step of the metallization process consists in autocatalytic growth of the fixed metal seeds on the DNA strand (Fig. 1d) by the addition of new metal ions (or metal complexes solution) and new reducing agent solution.

The principle of this autocatalytic process is that metal complexes or ions from solution are preferably reduced on already reduced metal nanoclusters (the seeds) fixed on the DNA strands. Here, it should be noted that this autocatalytic cluster growth can be generalized to metal nanoclusters fixed on DNA strand by any other method. Indeed, an effective metallization has been reported on ex situ prepared gold nanoclusters successively fixed on the dsDNA (i) by an appropriate chemical functionalization [21], (ii) by specially modified DNA construction [22], or (iii) simply by electrostatic interactions [23–25]. In this context, it is worth to quote the work of the Carell group on insertion in dsDNA sequence of modified bases to perform base-selective chemistry to conjugate metallic seeds. By this method, they inserted silver [26–28] or gold nanoclusters [29] selectively in the dsDNA

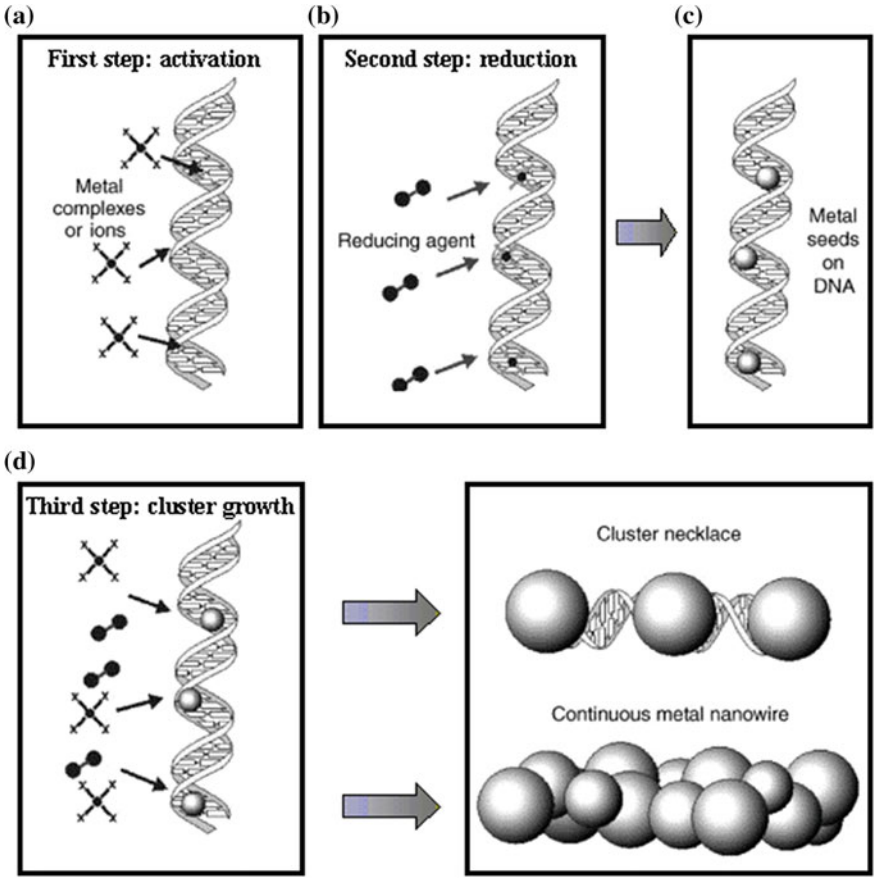


Fig. 1 Schematic representation of the different steps of the DNA metallization process. Adapted from Ref. [20]

sequence, then an electroless plating process (goldenhance) [30, 31] on such nanoclusters has been performed.

As mentioned above, different metals have been used in the metallization process. For the ion-exchange mechanisms on the dsDNA backbone, we can quote silver [13, 32], copper [33], or gold [34]. For the silver process, the obtained wires consisted in a chain of contiguous 30–50-nm Ag grains along the dsDNA backbone and the electrical measurements performed on such Ag necklace wires were not completely satisfactory. In a successive work, the same group improved the process by replacing the silver clusters growth with an electroless gold coating of the silver-loaded dsDNA molecules [19]. In this way, using silver ions as catalysts, conductive gold dsDNA-templated wires with widths ranging from 50 to 100 nm were obtained. This procedure can be generalized and the final metal coating does not necessarily have to use the same metal as the seeding one [19, 21, 35].

Concerning the intercalation mechanism of metal complexes between the DNA bases, the Pd or Pt complexes have been the more extensively studied. Indeed, the binding process of Pt(II) complexes to DNA is well investigated in the case of cisplatin (*cis*-[$Pt(NH_3)_2Cl_2$]), which is widely used as an anticancer drug [36]. It follows from these studies that when DNA is incubated with Pt(II) complexes such as cisplatin, the Pt(II) atom binds to one- or two-stacked DNA bases forming monofunctional and bifunctional DNA-Pt(II) adducts, respectively. The most favorable binding site for cisplatin to the DNA is the N_7 position of guanine, followed by the N_7 position of adenine [37, 38]. Indeed, the bases A, G, and C have exocyclic amine groups as well as ring amines, but it is the ring amines that act as Lewis bases. The Lewis base acidities differ from base to base, with the N_7 position of guanosine being the most basic. Other Lewis bases found in the nucleobases are N_7 of adenosine, N_3 of cytosine, and the deprotonated N_3 of thymidine or uridine. The amines are all soft ligands and as such preferably complex to soft metals such as Pt(II), Pd(II), or Ru(II). When the DNA is in double-strand configuration, the arrangement of the basis is controlled by π stacking and then the Lewis base sites available for coordination to the metal (Pd, Pt, etc.) are limited to the exposed portion of the nucleobases found in the major groove (the N_7 position of guanosine and adenosine). It is commonly thought that of these two sites, the N_7 of guanosine is the preferred one [38]. After these sites are occupied, the binding reaction proceeds more slowly and indiscriminately with other metal-binding sites of all bases [38–40]. Using this intercalation mechanism, Pd- and Pt dsDNA-coated nanowires have been obtained.

Finally, as an alternative way to DNA metallization, the photo-induced autocatalytic silver reduction has been reported [41]. The incident UV light with a wavelength near to the absorption maximum of the DNA bases (254 nm) induces the in situ reduction of silver ions that were preloaded onto the DNA samples. The bases act as light sensitizers for the Ag^+ and thereby induce the formation of metallic silver clusters along the DNA strands.

A global schematic view of the main works reported in the literature is presented in Fig. 2. Note that the conductivity of the obtained nanowires has not been measured in all reports. Generally speaking, these metallization processes of the DNA strands have been performed either (i) in solution and then the metallized DNA molecule is deposited on the substrate for the characterization purpose, or (ii) on the DNA previously deposited on the substrate.

The first case concerns, for example, the works reported by Harnack et al. [21] and Mertig et al. [42], who showed the formation of tiny platinum nanocluster necklaces consisting of well-separated clusters of 3–5-nm diameter with spacing from one to several nanometers.

On the contrary, Richter et al. [43], Nguyen et al. [44], Deng et al. [45], Dupraz et al. [35], and Ongaro et al. [23] have metallized DNA strands already deposited on the substrate. More in detail, Richter et al. fabricated continuous Pd nanowires with average diameters of 60–100 nm on DNA strands aligned on interdigitated gold electrodes with interesting transport properties, while Nguyen et al. [44] obtained conductive Pd nanowires with diameters in the range of 30–60 nm. On the contrary,

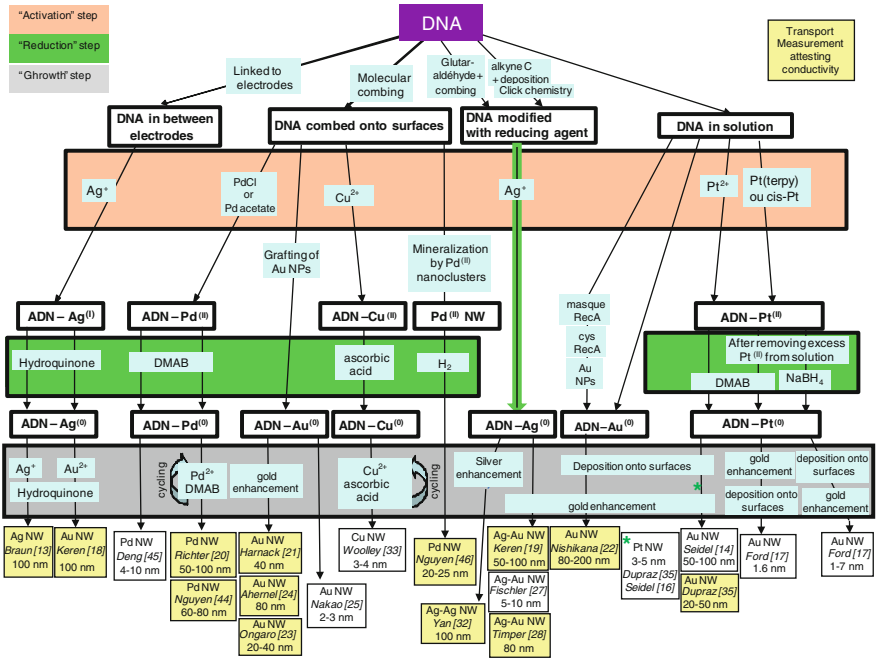


Fig. 2 Schematic representation of the main different pathways of the DNA metallization process. The *yellow boxes* represent the works where transport measurement has been performed

Deng and coworkers [45] reported very granular 30-nm Pd nanowires without any data about their conduction properties. Actually, both Dupraz et al. [35] and Ongaro et al. [23] started the metallization process in solution (seeds fixation) and successively stretched the metal-loaded DNA on the substrate. They used, respectively, Pt and gold nanoparticles as catalytic seeds, then they completed the metallization process by an Au electroless plating process. They both obtained DNA-templated Au nanowires (average diameters about 50 nm) with estimated resistivity of the order between 10^{-5} and 10^{-4} $\Omega \cdot$ m. At the time of writing, the thinnest conductive nanowires are about 20–25 nm in diameter [46].

At this point of our discussion, we should point out that among all the above-presented methods, only a few could be effectively and promisingly envisioned for nanocircuits' application. Indeed, the first condition that must be satisfied is that the obtained nanowires demonstrate good conducting behaviors. Then, as already noted, the metallization should be envisioned as the very last step of nanocircuits' fabrication since after this process all the recognition properties of the DNA molecules are completely lost. Finally, it is also crucial to be able to perform both effective and sequence-selective metallization where some parts of DNA scaffolds are not metallized (to avoid undesired electrical connections and shortcuts).

4 Sequence-Selective DNA Metallization

As mentioned above, in some cases, it can be desirable to define the parts of DNA strands to be metallized, while other parts are preserved. On this topic, we can quote three main studies which have been reported in the literature [18, 19, 22]. They are all based on the RecA protein properties. In vivo, the RecA protein is a central

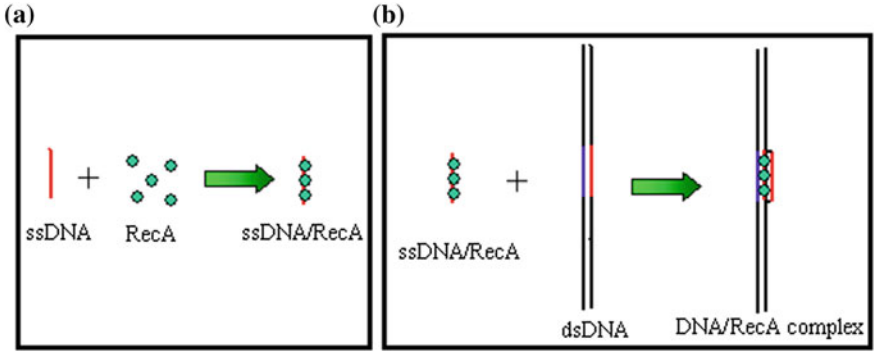


Fig. 3 Schematic representation of homologous recombination process that leads to binding of the ssDNA–RecA nucleoprotein filament at the complementary address on the dsDNA

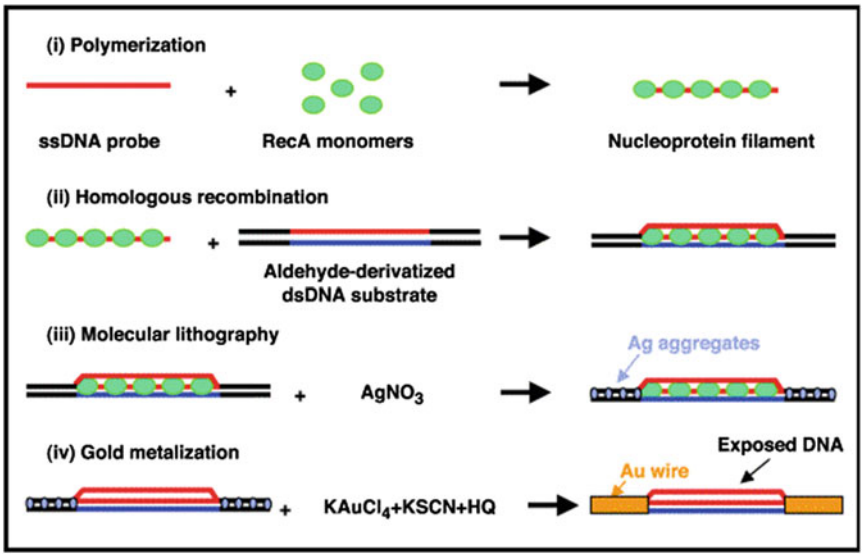
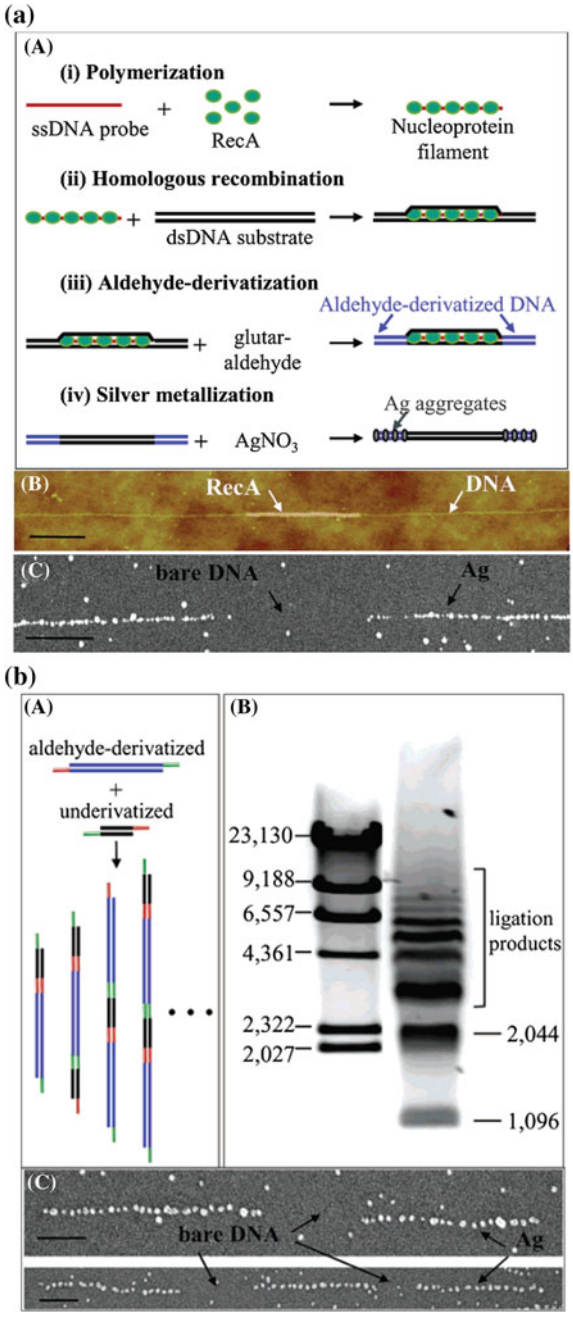


Fig. 4 Mechanism of sequence-selective metallization process. Thanks to the homologous recombination, the RecA protein acts as a sequence-specific resist for the creation of the silver seeds and successive gold metallization. From Ref. [18]


(a)
(A)
(i) Polymerization
ssDNA probe
+
RecA
Nucleoprotein filament
(ii) Homologous recombination
+
dsDNA substrate
(iii) Aldehyde-derivatization
Aldehyde-derivatized DNA
+
glutar-aldehyde
(iv) Silver metallization
Ag aggregates
+
AgNO3
(B)
RecA
DNA
(C)
bare DNA
Ag
(b)
(A)
aldehyde-derivatized
+
underivatized
(B)
23,130
9,188
6,557
4,361
2,322
2,027
ligation products
2,044
1,096
(C)
bare DNA
Ag

◄ **Fig. 5** **a** Selective metallization obtained by protection against aldehyde-derivatization of DNA using RecA as a sequence-specific resist. (*A*) Schematics of the protection reaction. (i) RecA monomers polymerize on a ssDNA probe molecule to form a nucleoprotein filament. (ii) The nucleoprotein filament binds to a dsDNA molecule at a homologous sequence. (iii) Incubation with glutaraldehyde leads to aldehyde derivatization of the substrate molecule in regions unprotected by RecA. (iv) Incubation of the patterned substrate DNA molecules in silver solution results in the formation of silver clusters in the aldehyde-derivatized regions, while the underivatized protected regions remain bare. **b** Selective metallization obtained by ligation of aldehyde-derivatized and -underivatized DNA fragments. (*A*) Schematic illustration of the ligation reaction (*B*) Gel electrophoresis analysis of the ligation reaction (*right lane*) run against a *ì-HindIII* digest marker (*left lane*). (*C*) SEM images of patterned metallization of DNA molecules obtained by ligation of alternating aldehyde-derivatized fragments and -underivatized ones. Adapted from [19]

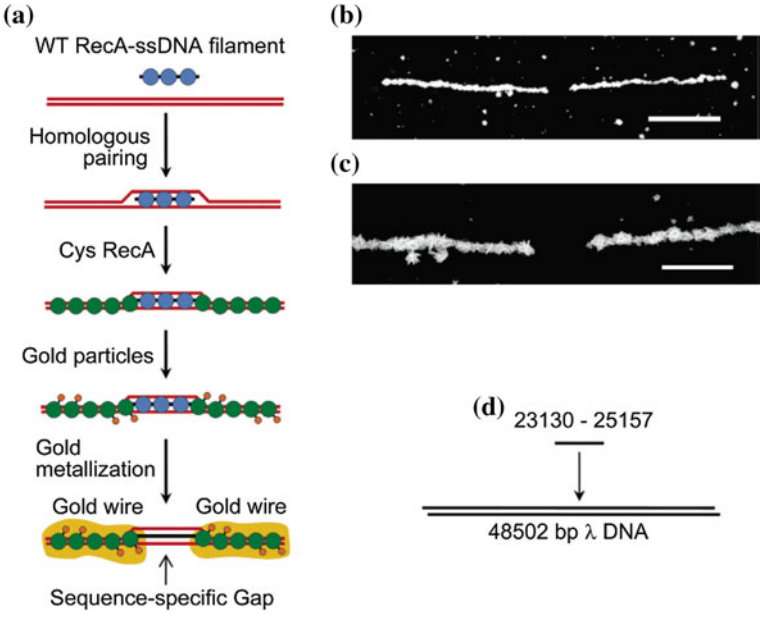


Fig. 6 Synthesis of conductive metal nanowires with a sequence-selective gap from complexes of single- or double-strand DNA and RecA protein. *Blue-* and *green-filled circles* indicate WT RecA and Cys RecA, respectively. The schema **a** shows how sequence selectivity is achieved: (i) Firstly, the wild-type RecA protein complexes with a copy of target ssDNA strand to be protected against metallization. Secondly, homologous pairing takes place and WT Rec A is inserted in the DNA strand. Thirdly, the so-obtained DNA is exposed to Cys RecA, bearing the Cys grafting for the gold nanoparticles. Then the gold nanoparticles are fixed onto the Cys RecA regions. Finally, the template-based gold particles were enlarged by chemical deposition to form uniformly metallized nanowires with the desired sequence-specific gap. **b** and **c** Show two scanning electron microscope images of two sequence- specific gaps at different magnifications. The scale bar is, respectively, 5 and 2 μm. **d** Indicates schematically the location of the ssDNA in λ scaffold. Adapted from [22]

component in recombinational DNA repair pathways and homologous genetic recombination (in Escherichia coli) [47]. In vitro, RecA protein demonstrates to promote the pairing and exchange of complementary DNA strands in reactions [48]. The mechanism is as follows: RecA catalyzes the pairing of single-strand DNA (ssDNA) with complementary regions of double-strand DNA (dsDNA). The RecA monomers first polymerize to form a helical filament around ssDNA (Fig. 3a). Duplex DNA is then bonded to the polymer (see Fig. 3b). However, it is worth to precise that RecA could polymerize onto dsDNA strands, too [49]. Thus, in 'in vitro' experiments after the polymerization onto ssDNA (Fig. 3a), the excess of free RecA should be removed to prevent an unspecific and undesired binding of RecA onto dsDNA [50].

In the framework of DNA-directed assembly of nanodevices, the RecA particular features have been used to differentiate a part of the DNA strand to achieve a sequence-selective metallization process. Indeed, the targeted sequence can be perfectly identified by the RecA-polymerized ssDNA fragment as in Fig. 3b. Then, the complex between the RecA–ssDNA polymer and the complementary regions of dsDNA can act as a mask for the metallization process. More in detail, the first report on sequence-specific metallization [14] suggested that this complex avoids the Ag^+/Na^+ ion-exchange blocking the formation of the Ag seeds on the targeted sequence. Consequently, the successive gold metallization is sequence selective since it takes place only where the metal seeds are present (see Fig. 4).

In a successive work [19], the same team showed that similar sequence-specific nanolithography can also be achieved by sequence-specific patterning of the local reducing agent (the glutaraldehyde). This patterning was performed either by ligation between aldehyde-derivatized and -underivatized DNA molecules or by sequence-specific protection against aldehyde derivatization by the RecA protein (see Fig. 5). Then, the sequence-specific patterning of the reducing agent is reflected by the sequence-specific creation of silver metallization seeds and successive gold metallization.

The third report on selective metallization uses the homologous recombination properties of the RecA protein, too. Its originality is to employ a modified RecA to act as a "linking factor" for sequence-specific fixation of gold nanoparticles [22]. Then, these gold nanoparticles are used as "seeds" for the metallization process. To be more precise, the authors use a genetically engineered cysteine derivative RecA protein (Cys-RecA) and, thanks to this derivatization, they are able to fix gold nanoparticles onto the Cys-RecA-DNA filament. Thus, they used separately cysteine-derivatized RecA and unmodified wild-type RecA (WT RecA) to complex different sequences of the DNA strand. Then, the fixation of the gold nanoparticles respects the targeted sequences bearing Cys-RecA-DNA and the successive metallization presents a sequence-specific gap corresponding to the unmodified RecA-DNA complex (see Fig. 6).

Finally, it is worth to say that also the method developed by the Carell group [26–29] could lead to sequence-selective conductive metallic nanowires since the metal seeds can be inserted onto a specific part of the sequences via the base labeling.

5 Applications of DNA Metallization in Nanoelectronics

In 2003, the Sivan group demonstrated the feasibility of DNA-directed approach for the assembling of a carbon nanotube field effect transistor [51]. In this work, some of the crucial ingredients of the DNA-directed vision were tackled and demonstrated, even if in a very simple and minimal geometry. More, in particular, the authors employed: (a) a selective placement of the nanotube on the DNA scaffold and (b) a sequence-selective metallization of the DNA strands. In this way, they were able to realize the electrical connection between the standard (lithographically defined) electrodes and the nanotube device. In both tasks (a) and (b), they exploited the sequence-specific homologous recombination of the RecA protein. They first anchored the single-wall carbon nanotube (SWNT) in the desired part of the DNA scaffold and then, after deposition on a substrate, proceeded to the selective metallization process. The SWNT/DNA linkage was performed in buffered solution by the molecular recognition of a streptavidin-functionalized SWNT toward biotin and by the antibodies' properties to link the biotin to the RecA/DNA filament, as schematized in Fig. 7.

Then, to fabricate the nanotube device, they stretched the SWNT/RecA/DNA assembly on a silicon substrate and performed the selective Ag/Au metallization process as described in Ref. [18]. One of the interesting features of this experiment is that even in this complicated configuration (presence of the SWNT, Streptavidin, biotin and antibodies species), the masking properties of the RecA are preserved and the "protected" segment of the DNA strand is not metallized. Finally, the DNA templated gold wires were connected by standard lithography electrodes to record the device characteristic. We note that DNA/RecA/SWNT complexes are randomly deposited on the silicon substrate and that the latter is also used as backgate. This implies that to fabricate the connecting electrodes, the deposited SWNT/RecA/DNA complex must be localized by imaging (AFM or SEM).

More recently, another approach has been proposed to fabricate a DNA-directed nanoelectrical device. In the report of the Winfree group [52], a DNA origami has been used as a nanobreadboard for arranging SWNTs as schematized in Fig. 8. Here, for device demonstration, the two SWNTS themselves ensure the electrical connections to the standard lithographically defined electrodes. More in detail, SWNTs were labeled by ssDNA to hybridize with hooks placed onto the origami. However, as already mentioned, when ssDNA spontaneously wrap around SWNTs, this ssDNA sequence is not readily available for the DNA-driven assembly. Thus, the authors used a particular engineered DNA fragment with a single-strand portion to wrap the SWNTs (the 40-T dispersal domain in Fig. 8a), while the part devoted to the hybridization is majorly dsDNA like with a 5bps LNA toehold in 3′ (see Fig. 8a). The role of such LNA toehold is to initiate hybridization with origami hooks inducing the successive 15-bps ssDNA strand displacement. The authors reported that using DNA toehold instead of LNA, one decreases dramatically the yield of the reaction.

In this way, the authors [52] managed to align ssDNA-labeled SWNTs along the lines of complementary hooks onto origami. Crossed SWNT geometries were

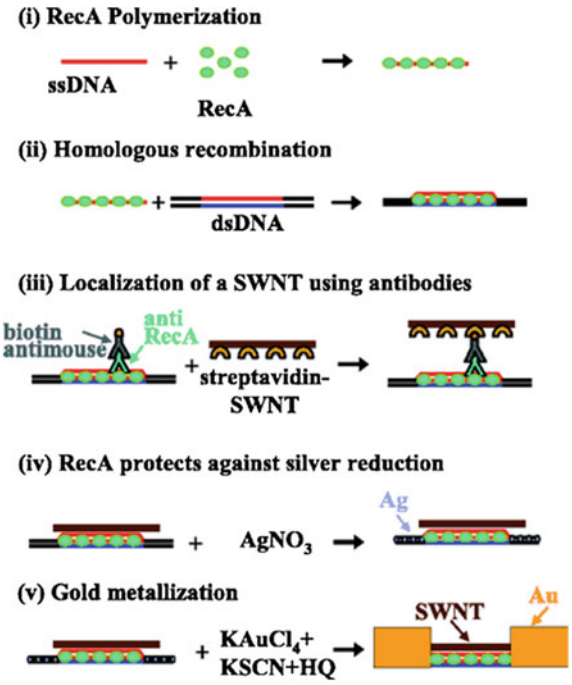


Fig. 7 Assembly of a DNA-templated FET and wires contacting it. Steps are as follows: (i) RecA monomers polymerize on a ssDNA molecule to form a nucleoprotein filament. (ii) Homologous recombination reaction leads to binding of the nucleoprotein filament at the desired address on an aldehyde-derivatized scaffold dsDNA molecule. (iii) The DNA-bound RecA is used to localize a streptavidin-functionalized SWNT, utilizing a primary antibody to RecA and a biotin-conjugated secondary antibody. (iv) Incubation in an $AgNO_3$ solution leads to the formation of silver clusters on the segments that are unprotected by RecA. (v) Electroless gold deposition, using the silver clusters as nucleation centers, results in the formation of two DNA-templated gold wires contacting the SWNT bound at the gap. Extracted from Ref. [51]

realized. In particular, their objective was to gate a semiconducting SWNT by a metallic SWNT using the DNA material present in the junction as gate dielectric. Indeed, by construction, the SWNTs are wrapped by ssDNA and the breadboard is also engineered to host the SWNT on different sides (see Fig. 8c).

If some criticisms are to be mentioned concerning this elegant work, they could be related to (i) the size of the DNA scaffolds with respect to the nanoobjects that are to be organized and (ii) the use of inter-SWNT DNA as gate dielectric material. Concerning the first point, the choice of arranging several hundred nanometers of SWNTs is probably dictated by the will of connecting these SWNTs by standard e-beam lithography and it is not very important since other scaffolds could be envisioned. In addition, this type of configuration could be of interest for relative positioning of nanoobject at the nanoscale and that longer objects like SWNTs could serve as wiring with larger electrical connexions. This type of approach has also been proposed by the group of Torma [53]. More specifically, Eskelinen et al.

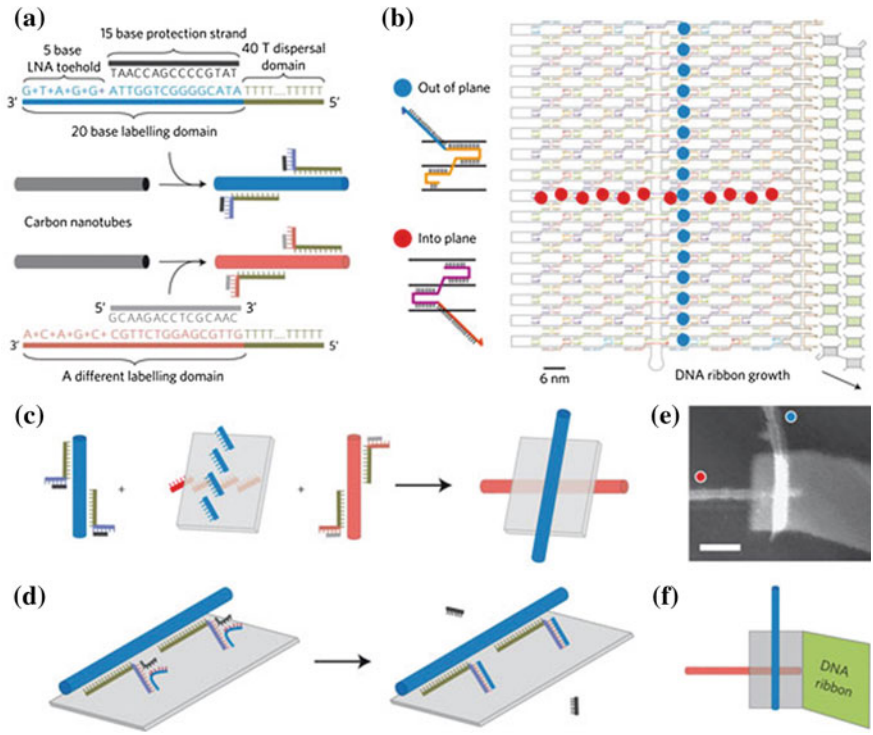


Fig. 8 Overview of cross-junction assembly. **a** ssDNA/SWNTs hybrids differ by linkers for which the labelling domains have different sequences. To distinguish them, SWNTs labeled with one sequence have been colored *red* and those labeled with the other, *blue*. Dispersal domains bind linkers to SWNTs; labeling domains project into solution. **b** A 7-kb-long scaffold strand (*grey*) and ssDNA staples (multicolored) form a rectangular origami template. Adapter strands (*brown*) on the right edge of the origami serve as nucleation sites for growth of a DNA ribbon (*green*/*grey tiles*). *Red* and *blue dots* indicate a pattern of hooks projecting from the origami. The *insets* show how staples are modified to carry hooks complementary to ssDNA/SWNT labeling domains of corresponding color; the scaffold is *black*. *Red hooks* project into the plane; *blue hooks* project out. **c** *Red* and *blue* ssDNA/SWNTs are mixed with a DNA template. They self-assemble sequence specifically with programed orientations, *red ssDNA/SWNTs* horizontally and *blue ssDNA/SWNTs* vertically. **d** The toehold on a linker initiates binding to a hook, leading to branch migration and release of the protection strand. Ribbons are not shown in c and d. **e** A typical AFM height image of a cross-junction on mica under buffer; *red* and *blue dots* indicate ssDNA/SWNT type. Scale bar, 50 nm. **f** Schematic interpretation of **e** highlighting the relationship of origami, ribbon, and SWNTs. Extracted from Ref. [52]

[53] reported a similar (but simpler) method based on streptavidin–biotin recognition as schematized in Fig. 9.

In the work of Eskelinen et al., first biotins are fixed both on the SWNTs and on the origami via biotinylated-ssDNA (respectively, via origami design and thanks to the ssDNA wrapping around the SWNTs, as shown in Fig. 9a, c). Then, streptavidin is linked via the biotins onto the origami (Fig. 9b) and serves as docking points for the biotin-coated SWNTs (Fig. 9d).

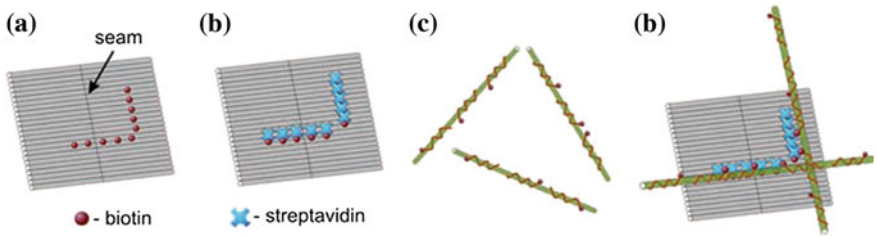


Fig. 9 Schematic diagram of CNT assembly on DNA origami templates using STV–biotin interaction. **a** As the first step, DNA origami structures with a certain pattern of biotin modifications were fabricated. **b** After that, streptavidin was assembled on the origami structure to define the binding sites for CNT attachment. Finally, **c** CNTs wrapped with biotin-modified ssDNA **d** were immobilized on the origami templates. Extracted from Ref. [53]

The main difference in these two reports is that in Maune's approach [52], it is possible to choose different sequences of the "hook" onto the origami. Thus, it is possible to assemble different kinds of nano-objects using different sequences. On the contrary, in the method presented by Eskelinen [53], the linkage is ensured by streptavidin–biotin recognition and another kind of linkage should be found if it is necessary to relatively position different nanoobjects.

6 Conclusion

The demonstration of completely DNA-directed self-assembled circuits is, at the time of writing this overview, still to be done. The knowledge and mastering of the different steps needed for the implementation of such a demonstrator are already reported in the literature and it is now a matter of multidisciplinary will and teams to accomplish the task. Finally, for such a still open and exploratory research domain, new findings are expected to further enlarge the present vision and generate novel strategies for the long-term development of nanoelectronics.

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Evaluation of Leakage Current in 1-D Silicon Dangling-Bond Wire Due to Dopants

R. Robles, M. Kepenekian and N. Lorente

Abstract Molecular devices will be contacted by systems with increasingly reduced dimensions. The device will need to be held somehow, possibly on a solid surface, and electronic currents will be addressed to the device via some kind of 1-D interconnect of atomic size. The fact that the device is posed on a surface brings in perturbations and eventually malfunctions of the device. Semiconducting surfaces have been deemed to be good candidates for this molecular technology because they have an electronic gap that prevents current losses from the device plus their surfaces are full of directional chemical bonds that make them ideal to hold a molecular device. However, semiconductors are generally doped, intentionally or unintentionally. Here, we summarized our findings on how destructive the presence of dopants is on the working parameters of a possible device. In fact, instead of a molecular device, we choose an ideal 1-D surface interconnect made out of Si dangling bonds in an otherwise passivated Si(100)-H surface. The current lost into a doped silicon substrate from a surface-supported nanowire is evaluated using transport calculations based on the density functional theory. We considered two concentration limits: either a single-dopant nearby the wire or a massively doped system. Both limits yield qualitatively similar results, stressing the strong perturbation that a single dopant can exert on an atomic-size wire. Our calculations permit us to conclude that n-doped Si will be less leaky than p-doped Si.

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1 Introduction

Semiconductor surfaces are good candidates for supporting molecular devices because they have an electronic gap that prevents current losses from the device plus their surfaces present localized chemical bonds that make them ideal to attach a molecular device. However, semiconductors are generally doped, and dopants can be a source of nuisance to the operational conditions of the device. On the one hand, they are strong electron scatterers, perturbing transport properties in a very long-ranged manner, and, on the other hand, they can close the semiconductor's gap.

An interesting material to study the effect of dopants is silicon. Silicon-based atomic-size circuitry has been rapidly progressing from new proofs of concept of devices to single-atom quantum dots, based on the surface silicon dangling bonds (DBs) [1] and new structures formed by DB quantum dots with qubit capabilities [2]. Indeed, DBs on an otherwise fully passivated Si(100)-H surface are very interesting: Arrays of aligned DB have been shown to present specific electronic properties [3], and single atoms have been precisely positioned in atomically thin epitaxial circuits to create an atomic transistor [4]. Interconnects have an important role because they can drive electronic currents in and out molecular devices. Free-standing [5] or supported [6] silicon nanowires have been shown to be possible interconnects. Other types of nanowires, such as rows of DBs, are good conductors [7]. In this context, dopants can severely impair the capacity of holding the electrical current to the interconnect: The current may leak from the wire. In traditional transistor-based circuitry, the leakage of current through the gate dielectric is actively studied [8]. However, the new interconnects lead to another type of current leakage due to the coupling of the DB wires to their environment. This coupling perturbs the device in different ways. The dielectric difference between nanowire and the surroundings can reduce the electronic current in up to 50 % [9]. Additionally, the leakage of the electronic current away from the wire can seriously disrupt the original properties of devices and bring to a halt the recent extraordinary technological progress. Present nanowires can be either epitaxially fabricated [10] or crafted [3, 11–14] on H-passivated silicon surfaces. Dopants, among other factors, determine the final transport properties by fixing the Fermi energy [15, 16] as well as the amount of scattering from the surface into bulk states. Hence, DB atomic scale wires supported by a doped substrate will not be electronically "tight", leaking current into the bulk material.

In this chapter, we are going to evaluate how much current is leaked from an ideal DB wire, when dopants approach the wire at different distances. Two concentration limits are explored: the single-dopant and the massively doped limits. Both limits yield qualitatively similar results, stressing the strong perturbation that a single dopant can exert on an atomic-size wire. Our calculations permit us to conclude that n-doped Si will be less leaky than p-doped Si. For the low bias at which these nanodevices will operate, leakage currents will be less than 10 % for n-doped Si substrates, and 20 % for p-doped ones.

2 Computational Details

Non-equilibrium Green's functions (NEGF) based on the density functional theory (DFT) calculations [17] are used to compute the electronic current through different surface wires as performed in Ref. [18]. Currents are evaluated from the transmission function, $T(E, V)$, between electrodes for an electron of energy E and a bias V following Landauer's equation [19]:

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} T(E, V)[f_R(E) - f_L(E)]dE. \quad (1)$$

where $f_R(E)$ $(f_L(E))$ is the right (left-)-electrode Fermi occupation function. We further simplify the current I calculation using the zero-bias transmissions. Here, a surface 2 × 1 unit cell includes a single Si(100) dimer and the slab supercell structure contains 8 bilayers in the direction perpendicular to the slab. The transport direction breaks translational invariance, and three different regions of the circuit are considered: (*i*) semi-infinite left electrode, (*ii*) contact region, and (*iii*) semi-infinite right electrode, as can be seen in Fig. 1. In order to evaluate the current leakage or, in other words, the fraction of current that leaves the confinement of the considered wire, we assume different atomic constructions of each region because, depending on whether dopants are included or not, the transport properties will be very different. A DB wire is built by removing one of the two hydrogens of the single dimer of the unit cell. Each of the three regions includes 4 dimers in the transport direction [18]. In order to simplify the numerical treatment, we have performed spinless calculations. Hence, the electronic structure of the studied DB

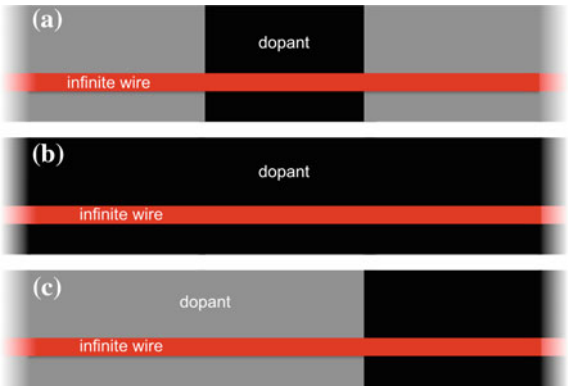

Fig. 1 Scheme for the atomic structures that held a wire over three different Si surface regions: two semi-infinite electrodes and a central connecting region between the electrodes. In **a** only the central region is doped, in **b** there are dopants in the three regions, and in **c** dopants are found in two regions, one being the contact region

wire corresponds to the perfectly metallic one that has been previously studied [18, 20, 21] albeit unrealistic as more accurate calculations show [11, 22–25].

Boron and phosphorous atoms replace a Si atom and create p-doped and n-doped regions, respectively, in Fig. 1. By placing the dopant at different distances from the wire, we can test the extension of the effect of the dopant in the current leakage. In order to avoid the reconstruction of the wire into a distorted one [11, 22–25], we use the coordinates of the passivated surface. In Fig. 1, we see three different combinations: (*a*) only the contact region (*ii*) is doped, (*b*) there are dopants in the three regions, or (*c*) the dopants lie in two regions, one of them being the contact region (*ii*). These combinations allow us to calculate different currents. The system of Fig. 1c contains an undoped electrode such that for low bias the only conduction channels belong to the nanowire. In this case, the current is entirely held by the DB wire since there is no other possible conduction path for the electrons entering the undoped electrode. This setup acts like a filter that selects the electrons that flow through the DB wire as the only ones forming the current. We call this contribution I_{filter}. In Fig. 1b, there is no restriction and holds a total current I_{total} that is composed of a dopant current contribution I_{dopant} and the DB wire contribution I'_{filter}. In Fig. 1a, the current is confined to the nanowire except where the transport channels are perturbed by the presence of dopants. This is the contact region where an extra contribution I_{impurity} can be found. Setups (*a*) and (*b*) are the same setup in two different doping limits: the single impurity or dopant limit for case (*a*) and the massively doped case (*b*). In the absence of dopants, the current will just be the full nanowire's current that we take as the current reference, I_{ref}, since it is the maximum current the nanowire can convey. Then, the leakage current will be $I_{\text{leakage}} = I_{\text{ref}} - I_{\text{impurity}}$ for (*a*) and $I_{\text{leakage}} = I_{\text{ref}} - I_{\text{filter}}$ for (*b*) and (*c*).

3 Results

A key quantity in our calculations is the electron transmission, $T(E, V)$, at a given energy, E and for a system bias, V, see Eq. (1). Figure 2 shows the transmissions at zero bias. Here, we assume that the interconnects are long enough to present a minimum electric-field effect, even if the biases get substantial. In the first panels of Fig. 2a, b, we find the results for B-doped substrates, and on (*c*) and (*d*) for P doping. As the impurities move away from the wires, the transmission changes, but within the used distances (15, 9.5 and 4 Å), the qualitative behavior is the same.

Figure 2a for a single impurity and (b) for a massively doped substrate, shows that for B impurities the negative-energy transmission is very affected. This is due to the interaction of the DB wire's electronic structure with the energy levels of the B ion itself. At positive electron energies, there is also substantial damaging of the transmission and indeed a full transmission channel disappears as our transmission eigenchannel analysis [26] shows. For P impurities, (*c*)-single impurity and (*d*)-many impurities, the higher-energy levels of the impurities lead the main effect to positive

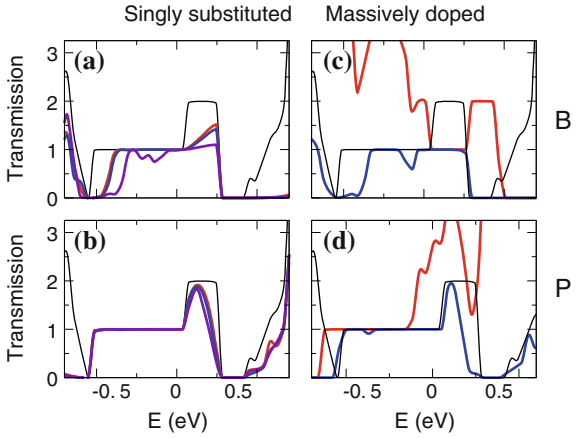

Fig. 2 Electron transmissions as a function of electron energy. In the absence of dopants, the transmission is shown in black. **a** Single substitutional dopant made by a B-atom located at 15 Å (*red curve*), 9.5 Å (*blue curve*), and 4 Å (*mauve curve*) underneath the nanowire. **b** Single substitutional P-atom for the same distances and color code as in (**a**). **c** Massively doped system with B-atoms in the left electrode plus contact region (*blue line*) and also in the right electrode (*red line*), the dopants are located at 4 Å underneath the nanowire. **d** Same as (**c**) but using P-atoms

energies. Indeed, P ions perturb the transmission less than B ions because the initial impurity levels lie further away from the Fermi energy. Hence, a lower leakage current for devices adsorbed on n-doped samples is expected. Blue curves correspond to setup (*b*) and red to (*c*), they are then the nanowire transmission and nanowire plus dopant transmission, respectively. A lot of information can be gleaned by studying the electronic levels of these systems. By computing the energy bands in a fully periodic system, we can obtain these energy levels. And indeed we obtain that the cause of the current leakage is the mixing of DB states with bulk states. In this way, DB states are not confined to the substrate anymore, and an electron transmitting through the surface DBs has a finite probability of ending up in the bulk material.

We compute the leakage current from the current expression, Eq. (1). Figure 3 shows the leakage current normalized to the current of the undoped wire. One of the main conclusions of this figure is that the percentage of leakage current is largely independent of the dopant concentration. This can be easily rationalized by the specificities of the system under consideration: the quasi one-dimensionality of the interconnect will make any perturbation as very strong, disrupting the conduction of the single channel. To this respect, the dopant-wire distance should play an important role. In order to check this, we have computed different leakage currents for different distances. The effect can be seen by comparing the two graphs on the left and the right of Fig. 3: as the dopant concentration near the wire decreases, the leak diminishes with single or many dopants yielding basically the same results. Hence, a single dopant located within tens of Ångströms of a DB wire is enough to cause a substantial mixing of the DB wire's electronic structure with the substrate's

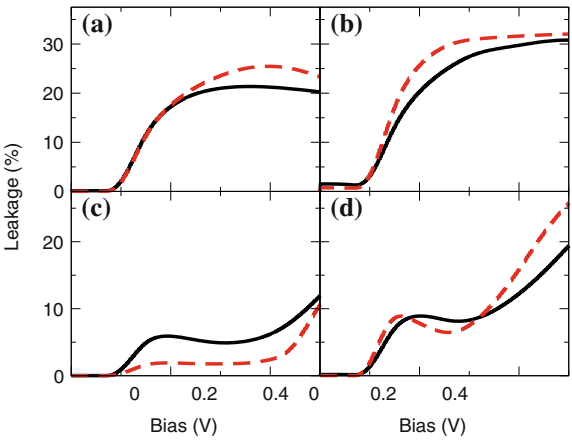

Fig. 3 Leakage current in % of the total current that the DB wire can hold. **a**, **b** For a B-atom replacing a Si atom 4 and 15 Å below the DB wire (*full line* single-dopant limit, *dashed line* massively doped limit). **c**, **d** For a P-atom 4 and 15 Å into the Si bulk as in (**a**, **b**)

one, leading to most of the expected leakage in these systems. It is noteworthy that B has a more sustained effect on the current leakage than P. Our calculations permit us to estimate that P-doped substrates can hold surface atomic wires with a current leakage of less than 20 %. At lower biases, this figure improves to less than 10 % due to the absence of bulk states near the Fermi energy. Due to the low-lying electronic levels of B ions, the current leakage in B-doped substrates is quickly in the range of $\sim 20 - 30\%$.

4 Summary and Conclusions

The current lost into a doped silicon substrate from a surface-supported nanowire is evaluated using transport calculations based on the density functional theory. The calculations are performed for an infinite non-periodic wire for various types of dopants. Two concentration limits are explored: the single-dopant and the massively doped limits. Both limits yield qualitatively similar results, stressing the strong perturbation that a single dopant can exert on an atomic-size wire. Our calculations permit us to conclude that n-doped Si will be less leaky than p-doped Si. For the low bias at which these nanodevices will operate, leakage currents will be less than 10 % for n-doped Si substrates and 20 % for p-doped ones.

Acknowledgments Authors would like to thank the European Union Integrated Project AtMol for financial support.

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Direct Integration of Carbon Nanotubes in Si Microsystems

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Abstract The integration of nanomaterials such as carbon nanotubes (CNTs) into microsystems is highly desirable, in order to make use of the unique nanomaterial properties in real devices. However, the CNT-to-microsystem integration is challenging to implement in a manufacturable, cost-effective industrial process. This text presents our work towards a process for making complete CMOS/MEMS systems with integrated CNTs. We demonstrate the feasibility of the process, using room-temperature processing, low-cost equipment and consumables, and electrical control with automation possibilities. CNTs are directly integrated at the desired positions in the Si microsystem, forming closed Si/CNT/Si circuits. An applied electric field during manufacturing ensures that the CNTs forming those circuits are well defined, thin and straight. We explore different designs with the aim to obtain uniform and well-defined CNT synthesis conditions and show that simplified designs can perform comparable to more complex ones. The Si/CNT/Si circuits obtained can show rectifying (Schottky-like) or near-ohmic behaviour. Gas sensing possibilities are demonstrated, indicating the possibility of monitoring ageing/fermenting of food. Functionalization of CNTs is demonstrated, using thermal evaporation of Sn and Pd, opening for selective and sensitive sensors for various gases and analytes. Detailed microscopic characterization of the obtained CNTs is presented.

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1 Introduction

Carbon nanotubes (CNTs) are materials with unique electronic, mechanical, thermal and optoelectronic properties. CNTs, together with graphene, are often termed "the strongest existing materials", with the highest known tensile strength and Young's modulus of any material [1, 2]. They have excellent thermal conductivity [3]. Their electrical properties are highly dependent on their structure: Different *chiralities* render metallic or semiconducting materials, respectively [4]. Metallic CNTs are capable of carrying high current densities [5]. The one-dimensional nature of CNTs renders all the material properties highly anisotropic. This can be exploited technologically, and it makes CNTs ideally suited as model systems for low-dimensional physics. CNTs exist as single-wall (SWCNT) and multi-wall (MWCNT) CNTs. MWCNTs (consisting of concentrically arranged CNTs) with one or more metallic CNTs will behave as metallic. Furthermore, the small diameter of CNTs ($\sim$nm to $\sim$tens of nm) implies that they have a huge surface-to-volume ratio.

These diverse, unique properties of CNTs make them promising candidates for a variety of applications in nanoelectronics and nanoelectromechanical systems (NEMS) in devices such as ultrasensitive gas sensors, optoelectronic devices and field-emission-based devices [6–10]. CNTs can also be an electron channel in transistors, potentially enabling miniaturization beyond the limit predicted for Si processing [11].

For all such applications of CNTs as functional material in a device, the integration of the nanomaterial into a microsystem is essential in order to access and make use of these nanostructures [12]. The ultimate goal is to combine CMOS and MEMS with CNTs on a single manufacturing platform, thus combining sensing, processing and actuating functions in a single chip. Normal CNT synthesis processes take place at high temperatures (700–1000 °C), using techniques such as arc discharge, chemical vapour deposition (CVD) and laser ablation [13–15]. Such high process temperatures imply that on-chip synthesis cannot easily be done without destroying CMOS circuits and MEMS structures. A normal requirement for CMOS compatibility is that post-processing should not exceed 300 °C, or up to 400 °C for short time periods. As an alternative to on-chip CNT synthesis, CNTs can be manufactured in bulk with subsequent integration into CMOS/MEMS microsystems. However, techniques for patterning, nanomaterial manipulation and bonding at nanoscale are not compatible with low-cost, high-volume production [16]. Manual transfer of individual CNTs and welding to microstructures by ion-beam (or electron-beam) metal deposition is demonstrated as a feasible laboratory-scale manufacturing method [17], but it requires serial processing in high-cost equipment. It is therefore not scalable to a low-cost industrial manufacturing process. Integration schemes such as solution processing (dispersed CNTs) [18] or dielectrophoresis [19, 20] are more aligned to low-cost, high-volume manufacturing.

However, they give little possibility for achieving single-nanotube connections with good electrical contact to electrodes. Solution processing results in random CNT networks. Dielectrophoresis allows alignment of CNTs, but subsequent metallization steps are needed to achieve electrical contact. An alternative method is to synthesize CNTs on separate wafers (in a high-temperature process), with subsequent wafer-level transfer to the active CMOS/MEMS wafer [21]. Whereas this approach has proven successful to produce device demonstrators, it relies on a number of process steps, including patterning and metallization.

On-chip synthesis of CNTs was first proposed by Englander et al. [22] and Christensen et al. [23] in 2003, demonstrating local synthesis of CNTs through localized resistive heating on purpose-made microstructures with a deposited catalyst layer. These Si structures are suspended for thermal isolation purposes and act as growth structures: The microstructures are locally heated by a current, maintaining the bulk of the chip at ambient temperature. A carbon-containing gas is introduced, and carbon nanotubes grow in a CVD-type process. The direction of CNT growth is guided by an electric field, controlled by the voltage applied to the microstructures. Thus, CNTs can be directly integrated as part of closed circuits, and the number of CNTs closing a connection can be monitored through electrical measurements during the experiment. Similar approaches have been used also by other groups [24], also using metallic growth structures [25].

This text presents the work of our group at Buskerud and Vestfold University College, Norway; aiming towards a wafer-level, room-temperature, low-cost CMOS/MEMS—compatible process for direct integration of CNTs into Si microsystems. We have demonstrated that the synthesis process, as sketched above, can be controlled through electrical measurements only [26], allowing for implementation in an automated industrial setting, and scalable to wafer-level manufacturing. Using low-cost consumables and rapid processing at ambient temperature ensures the low cost crucially important for such a process to be industrially feasible. In this text, we also present design considerations for the Si microstructures, aiming at a well-defined and measureable synthesis temperature. We further present our detailed findings of the effect of an applied electric field on CNTs, which effectively works as a sorting mechanism for circuit manufacturing. Furthermore, electrical properties in terms of circuit IV-curves, as well as initial functionalization of the locally grown CNTs, are presented.

Our process is particularly aiming at applications where the combination of nanomaterial functionality and low system cost is essential. An example is gas sensing for monitoring the ageing process of food, where low cost is crucial for technology to be implemented at the consumer level. Our aim is an integrated device as sketched in Fig. 1. Whereas CNTs can be used in their virgin state, they can also be functionalized to increase the sensitivity and selectivity to various gases and analytes.

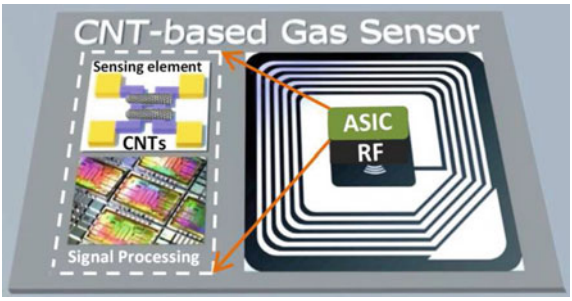

Fig. 1 Conceptual illustration of a complete CNT-based gas sensor using carbon nanotubes as sensing elements implemented directly into a MEMS/CMOS chip with RF circuitry for direct communication with the consumer

2 Experimental

2.1 Design

Single crystal silicon microstructures for localized CNT synthesis were designed and fabricated, using the commercial process SOIMUMP (Silicon-On-Insulator Multi-User MEMS Process). Previously, our group has used polysilicon structures in the PolyMUMP (Polysilicon Multi-User MEMS Process) [12]. This previous demonstration on polysilicon structures (also used as comparison in the present work) is important as model structures for simulating a process that integrates CNTs on CMOS/MEMS at low cost. Single crystal structures using silicon-on-insulator (SOI) are a more well-defined test vehicle, eliminating the influence of grain boundaries on conductivity. This feature is important, since the temperature in the CNT growth structure is estimated through the resistive power dissipation. An uncertainty in conductivity will give an uncertainty in obtained microstructure temperature, being perhaps the most important experimental parameter. The SOIMUMP also gives the possibility to design a hole in the chip. Such a hole allows for transmission imaging of CNTs crossing the hole using S(T)EM (scanning electron microscope with transmission imaging option), revealing far more details than scanning electron microscopy (SEM) using secondary electron imaging. Both SOIMUMPs and PolyMUMPs use standard microfabrication techniques, as specified in http://www.memscap.com/products/mumps. In both cases, the device layer is doped with phosphorus (*n*-doping).

Figure 2 shows an example of such a microstructure, with two microbridges. The primary bridge is heated resistively and is designed with a wider central part for a more uniform temperature distribution and with a meandering part to account for the thermal expansion occurring during local CNT synthesis.

In a study on the impact of microheater design, four different designs were made, and microscope images of the resulting designs are shown in Fig. 3. All have a through-hole for transmission imaging in S(T)EM, and all have a wider central part

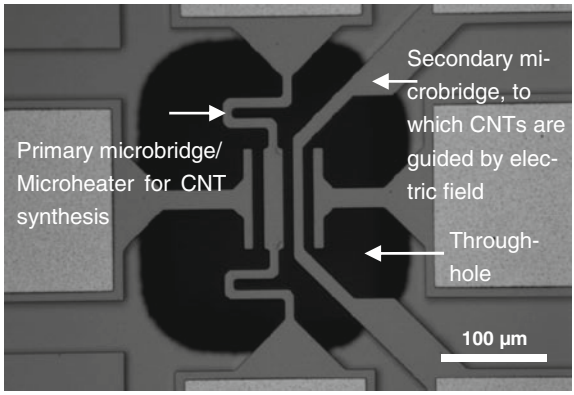

Fig. 2 Micrograph of SOI microstructure for localized CNT growth

(20 µm, as opposed to 10 µm for the supporting beams). Designs 1 and 2 have springlike beams as described in the previous paragraph. Designs 1 and 3 contain two additional narrow beams for four-point resistance measurements, thus being a measurement of the temperature of the growth structure. The beams are narrow to minimize the heat leakage, as such a heat leakage will give a lower temperature in the microheater than estimated. Four-point measurements of the resistance in this part of the structure with fairly uniform temperature give a far more reliable

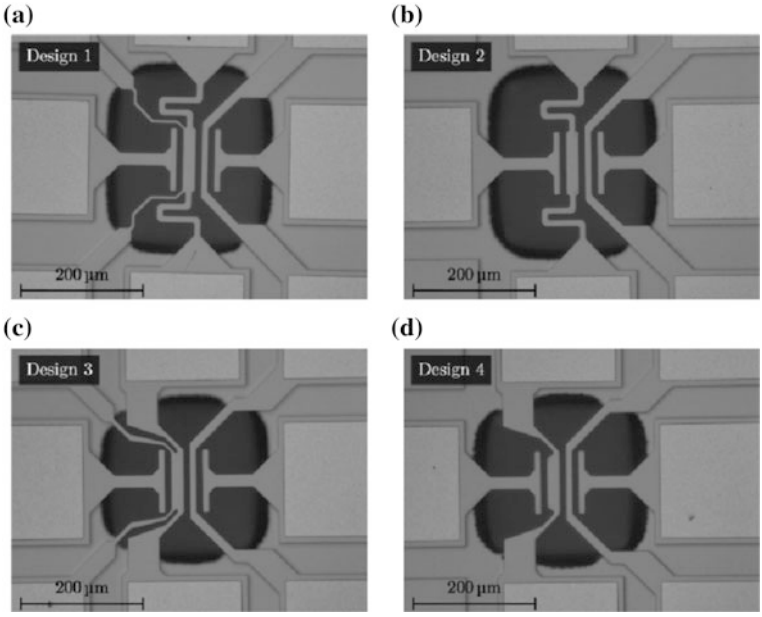

Fig. 3 Four different designs of microstructures

temperature measurement than the two-point measurement done over the whole microbridge (including supporting beams, wire bonding pads and connections), since the latter method implies integrating over structures with large temperature variations. However, two-point measurement is the preferred method from a process control perspective, since it requires fewer connections and simpler structures. If the proposed method is to be scaled up to wafer-level manufacturing, it will be crucial to keep the number of electrical connections per device at a minimum level and equally crucial to simplify structure geometries. Comparing two-point and four-point measurements for verification of the two-point measurement method is therefore important.

For SOIMUMPs, the doping concentration at the surface is of the order $10^{20} \times \text{cm}^{-3}$ [27] and decreases with distance down into the device layer (in our case: the microbridges). This doping profile arises from the solid-state dopant diffusion following deposition of a phosphosilicate glass layer and annealing. By comparison, the doping level of PolyMUMPs is more uniform, in the order of $10^{20} \times \text{cm}^{-3}$.

FEM simulations give the relation between the current flowing in a specific microstructure design and the temperature distribution in the microstructure. The doping profile of the Si structure is modelled as a two-layer structure: an upper, heavily doped 1-μm-thick layer, and a "bulk" part (the remaining 9 μm thickness of the single crystal device layer) with more than four orders of magnitude lower doping concentration. The modelled doping profile is in accordance with the sheet resistance measured in [27]. The simulation model takes into account the temperature-dependent electrical conductivity of the two modelled Si layers, the temperature-dependent thermal conductivity and thermal expansion, as well as the Thomson effect (charge carriers transporting heat).

2.2 Synthesis and Characterization

A thin layer (1–3 nm) of Fe is thermally evaporated on the Si microstructure, to act as catalyst for CNT growth. This is done in a mask-free process. The layer is sufficiently thin to avoid short circuiting of the structures, and the Fe film forms nanoparticles upon thermal annealing of the primary microbridge [28]. The growth structure is heated in inert atmosphere (Ar) by passing a current through it. At the desired growth temperature, the heated microstructure is exposed to a flow of C_2H_2 and Ar, while an electric field is applied between the two microstructures in the design. Figure 4 shows a sketch of the growth process. The current between the two microstructures is monitored during growth, a jump in this current revealing a CNT closing the circuit between the two structures.

The structures with integrated CNTs are inspected using SEM, both in secondary electron mode and in transmission imaging mode using a S(T)EM (Hitachi S5500). IV-curves, showing the current flowing in the CNTs connecting the two microbridges as a function of the voltage applied between them, are measured.

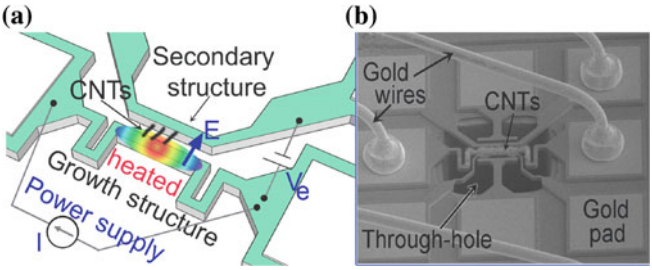

Fig. 4 **a** Sketch of the CNT growth process. **b** Micrograph showing electrical connections

As a preliminary test for the applicability of our approach to fabricate a sensor for monitoring the ageing process for food, a system with CNTs connecting microbridges was exposed to alternating CO_2 and Ar atmosphere. The resistance of the system was measured in a Wheatstone bridge configuration (the measured signal thus being a voltage signal).

In order to demonstrate the possibility to functionalize our CNTs, thermal evaporation of metals such as Sn and Pd was done on systems with CNTs directly integrated.

3 Results and Discussion

3.1 Design

The simulated electrical resistance for the four different microbridge designs is shown in Fig. 5. The shape of the curves reflects the temperature-dependent resistivity of doped silicon: Increasing temperature leads to decreasing carrier mobility (hence increased resistivity) due to increasing phonon scattering, until a

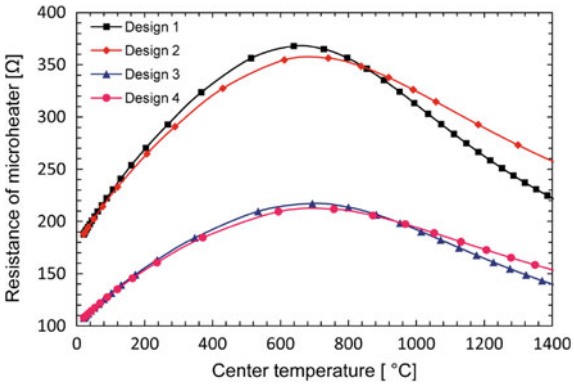

Fig. 5 Simulated resistance of microheaters as a function of centre temperature

crossover where the excitation of electron–hole pairs in intrinsic silicon (density increasing with temperature) gives decreasing resistivity with increasing temperature. The centre temperature of the microbridge during CNT synthesis can be obtained by measuring the microbridge resistance, using Fig. 5 as resistance-to-temperature conversion.

To verify the precision of the simulations in Fig. 5, the simulation results are plotted as resistance versus supplied heating power, and compared with experimental values, as shown in Fig. 6. The simulated values are found to represent the experiment well, both for 2-point and four-point measurements. The technique of temperature measurement through resistance measurement, also using the simplified 2-point measurement, is therefore found to be relevant. This implies that a system intended for large-scale manufacturing can have a simplified design without the additional beams for four-point measurements and with a reduced number of interconnections.

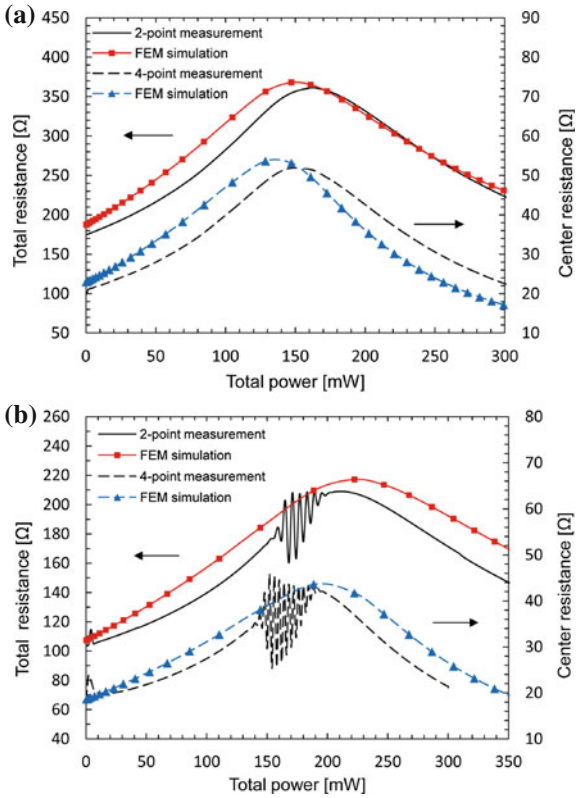

Fig. 6 Measured and simulated resistance of microheaters as a function of heating power. Two-point measurements represent the entire microbridge, whereas 4-point measurements represent the central part with fairly uniform temperature. **a** Design 1, **b** Design 3. The oscillations in the measured curve in (**b**) are caused by an artefact of the power control system

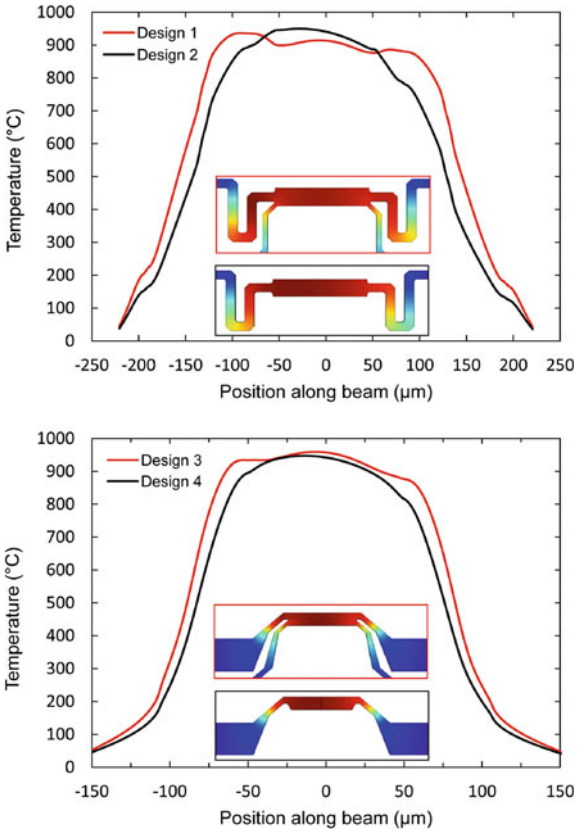

Fig. 7 Simulated temperature profiles for the four microheater designs

Figure 7 shows the simulated temperature profiles for the four different microheater designs, with a heating power supply corresponding to a maximum temperature of 950 °C. The temperature profile is quite uniform in the region of interest, with a temperature window of 38 °C (Design 1) to 106 °C (Design 4) for the central, wide part of the microheaters.

3.2 CNT Synthesis

Figure 8 shows a micrograph of a Design 4 microstructure after CNT growth, together with the simulated temperature profile. This is the design with the largest temperature variation (Fig. 7), and the temperature-dependent variations in CNT growth density can clearly be observed. This underlines the importance of microstructures with a uniform temperature, for predictable and uniform CNT growth. The three other designs, having more uniform temperature distributions, also exhibited a higher uniformity in CNT growth across the microheater.

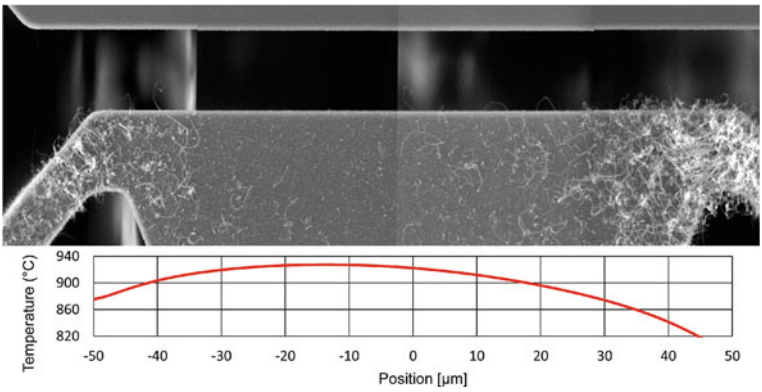

Fig. 8 Microheater (Design 4) after CNT growth, with simulated temperature profile

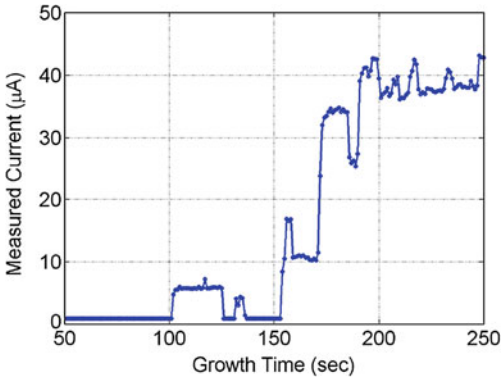

Fig. 9 Current flowing in CNT connections during the synthesis process

Figure 9 shows an example of the current measured between the two Si microstructures during the synthesis process. Positive steps in the current are observed when CNTs connect the two structures, forming a closed electrical circuit. Negative steps in this current are observed when connection(s) are broken. In the early time of the synthesis process, the connections are somewhat fragile, as seen in Fig. 9.

Figure 10 shows a typical image of resulting CNTs from our local synthesis/direct integration approach (in this case from a poly-Si growth structure). A large number of CNTs grow on the hot microstructures. Whereas most of these grow in a disordered fashion, resulting in curled structures on the Si microbridge, a number of CNTs are straight and actually close the gap between the two microstructures, as expected from the current–time measurement shown in Fig. 9.

Figure 11 shows high-magnification transmission images of individual CNTs, with diameters 40 and $\sim$8 nm, respectively. Three different contrasts appear (best seen in the 40 nm CNT), easily interpreted as a multi-walled CNT (MWCNT) with inner

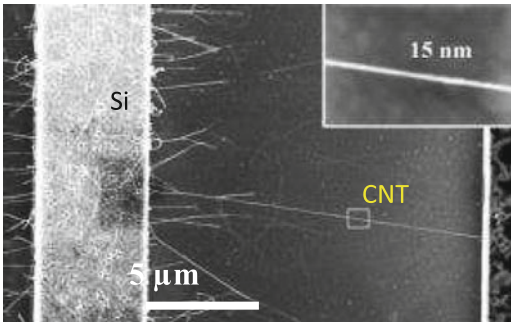

Fig. 10 CNTs grown on heated poly-Si microstructure

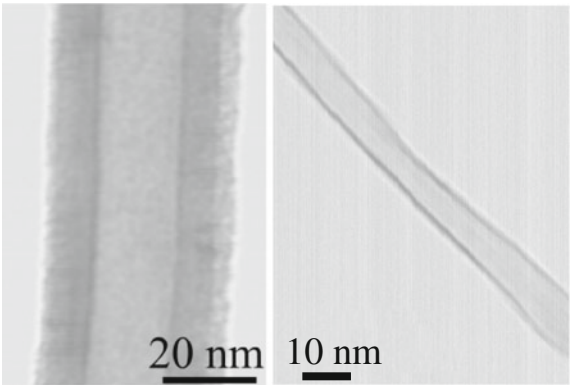

Fig. 11 Detailed view of individual CNTs, transmission image in S(T)EM

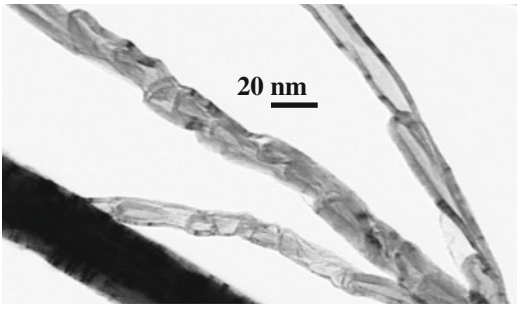

Fig. 12 CNTs showing defect structures, transmission image in S(T)EM

diameter given by the width of the bright core in the image, and the multi-wall thickness given by the width of the dark contrast. The outermost semi-bright feature may be disordered carbon deposits.

The CNTs produced in our method have a significant variation in degree of order. The micrograph in Fig. 12 shows an example of CNTs with high defect density. Such CNTs are observed when the synthesis temperature is lower than optimal.

3.3 *Effect of Applied Electric Field*

The CNTs closing the gap are the ones that contribute to an electric circuit and the ones that are of importance for, e.g. sensing applications. A detailed statistical analysis has been carried out on a large number of CNTs as observed by electron microscopy, correlating the CNT diameter with their straightness and orientation [29]. The CNT straightness is defined as the ratio between a straight line connecting the two ends of a CNT and the actual length of the CNT, as sketched in Fig. 13. This straightness parameter s thus may take the value $0 \leq s \leq 1$. The deviation angle is defined as the angle the straight line connecting the two ends of a CNT makes with the electric field set up to guide the CNT towards the secondary structure. Figure 14 shows the result from $\sim$500 CNTs analysed for one and the same growth sample, thus comprising all CNTs extending from the growth structure towards the secondary structure. It is clearly seen that all CNTs with diameters <5 nm are very straight and well aligned to the electric field. For CNTs with diameters >10 nm, the opposite observation is clear: Very few CNTs are straight, and there is rather a tendency for CNTs to bend back towards the original growth structure than for alignment with the electric field. CNTs with diameters 5–10 nm show a transition between these behaviours. These findings have been explained by an electrostatic and thermodynamic model, where the electrostatic model takes into account both the longitudinal *and* the transverse polarizability of CNTs [29].

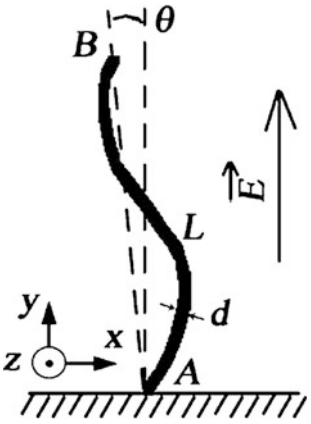

Fig. 13 Definition of the analysed parameters (s, θ). The straightness = AB/L, where L is the length of the CNT. The deviation angle θ is the angle between AB and the applied electric field. Figure reprinted from [29] with permission

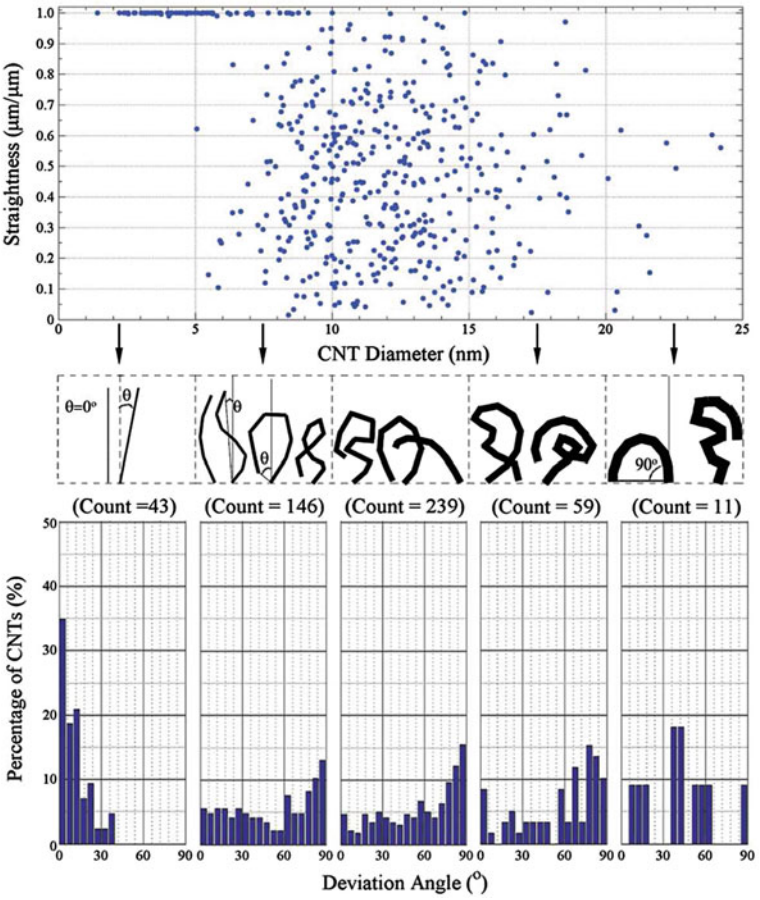

Fig. 14 Straightness and deviation angle of directly integrated CNTs. (*Top*) Straightness of CNTs (*s*) versus diameter (*d*); (*Middle*) Typical shapes of the observed CNTs; (*Bottom*) Distribution of the deviation angle (θ). Figure reprinted from [29] with permission

The local growth process in itself is not expected to produce a well-ordered CNTs as a bulk process with possibilities of subsequent refining. Figure 12 indeed shows such defect CNTs, grown at temperature below the optimal. Such conditions will naturally exist in the areas outside the hotspot areas for the microstructures for CNT growth. However, the diameter dependence on field alignment shown in Fig. 14 effectively ensures that the thin, straight CNTs are the ones that are guided towards the secondary structure and become part of a Si–CNT-based device.

3.4 Electrical Properties of Si–CNT–Si Systems

IV-curves (Fig. 15) show that the Si–CNT–Si system can have both rectifying and near-ohmic behaviour. Systems on the SOIMUMP platform (Fig. 15a) show either

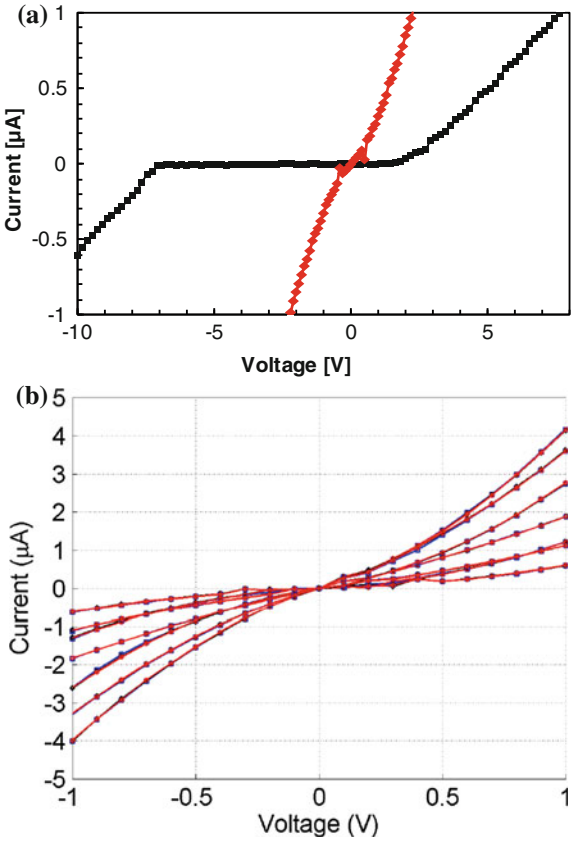

Fig. 15 IV-curves for Si–CNT–Si systems. **a** SOIMUMP microstructure, giving near-ohmic or rectifying (Schottky-like) behaviour. **b** PolyMUMP microstructure, giving near-ohmic behaviour. Note that the IV-scales are orders of magnitude different in (**a**, **b**)

a rectifying (Schottky-like) or a near-ohmic behaviour, whereas the systems on the PolyMUMP platform (Fig. 15b) show a more ohmic behaviour. These platforms differ in their doping level: The PolyMUMPs have a uniform, high doping level, whereas the SOIMUMPs have a decreasing doping level with depth in the device layer. CNTs can grow from different depth locations at the primary microbridge and connect to different locations at the secondary microbridge. We assume our CNTs to be multi-walled (as suggested by their diameters), hence metallic. Connecting to highly doped Si, an ohmic behaviour is expected, as shown in Fig. 15b. For lower doping levels at the junction, a Schottky-type metal-to-semiconductor junction is created. The circuit can then be modelled as two diodes connected back-to-back in series with a resistance [30].

An applied voltage higher than the reverse breakdown voltage of one of the diodes is needed for a current to flow in either direction. The near-ohmic behaviour observed for several structures is interpreted as a connection between MWCNT and

intermediately highly doped Si. Note that the deviations from linear, ohmic behaviour always result in slightly "S-shaped" curves, qualitatively resembling the shape of the Schottky-type curve as shown in Fig. 15a. In order to achieve true ohmic behaviour, higher doping levels for the Si structures should be used.

3.5 *Gas Sensing and Functionalization*

Figure 16 shows a demonstration of the capability of CNTs directly integrated in Si microsystems to act as a gas sensor, where we show that the Si/CNT/Si system changes resistance significantly whether the system is exposed to Ar or to CO_2 [31]. The ability to differentiate Ar and CO_2 is relevant for monitoring of ageing of food, since many food products are packaged in inert atmosphere, and CO_2 is a typical product of a fermentation process. The large voltage signals observed in Fig. 16 indicate the potential of the method.

The system used for obtaining the data in Fig. 16 consists of pristine CNTs integrated in the Si system. The sensitivity and selectivity to various gases can be enhanced through functionalization of CNTs. Figure 17 shows one of our early results in functionalization with tin oxide nanoparticles, using the approach of thermal evaporation of Sn. This is a straightforward experimental approach that does not expose the chip to high temperatures. Tin oxide is a relevant functionalization material, sensitive to several gases such as NO_x, CO, O_2, H_2 and NH_3. Similarly, we have functionalized our CNTs with Pd nanoparticles [32] using thermal evaporation, Pd typically being used for the detection of H_2. The result is shown in Fig. 18. As observed in Figs. 17 and 18, the nanoparticles appear to be fairly uniform in size and distribution along the CNT. For Pd deposition (Fig. 18), the nanoparticle diameter is in the range 1–2 nm. For Sn deposition (Fig. 17), the nanoparticle diameter is somewhat larger, and with a somewhat larger spread:

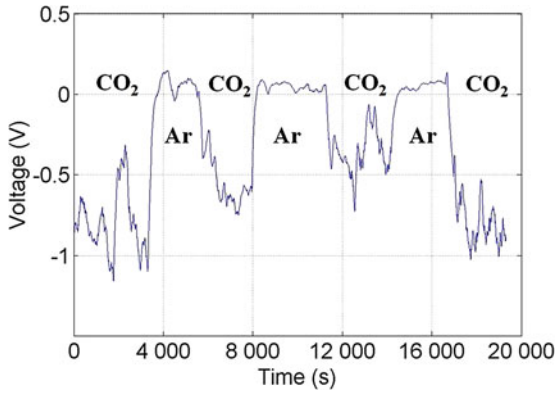

Fig. 16 Response of CNT-based gas sensor to Ar and CO_2. The voltage drops when CO_2 is introduced into the chamber, replacing Ar [31]. Figure reproduced with permission [31]

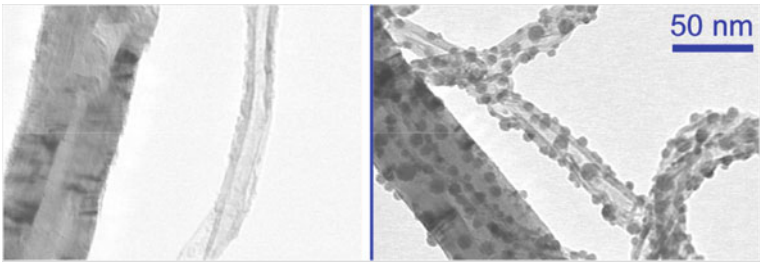

Fig. 17 *Left* A CNT before thermal evaporation of Sn. *Right* a CNT covered with tin oxide nanoparticles after thermal evaporation. Transmission images in S(T)EM

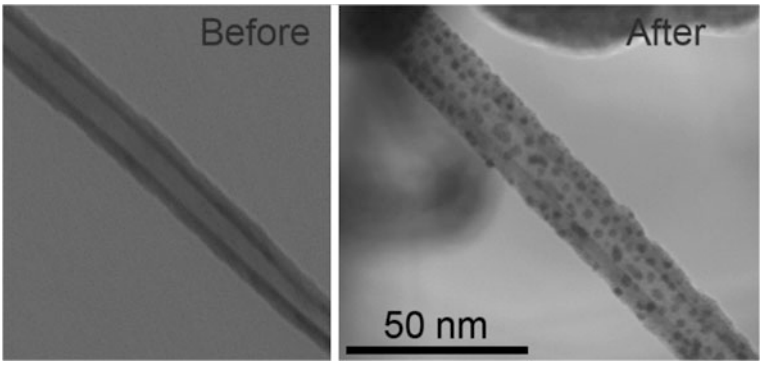

Fig. 18 *Left* A CNT before thermal evaporation of Pd. *Right* a CNT covered with Pd nanoparticles after thermal evaporation. Transmission images in S(T)EM. Figure reproduced with permission [32]

2–7 nm. As the Sn deposition takes place in a vacuum environment, it is likely to believe that the nanoparticles are deposited as metallic Sn, which is oxidized to tin oxide upon subsequent exposure to air. This oxidation will also naturally lead to an increased volume of the nanoparticles.

A defect-free CNT does not necessarily bond well to foreign elements. Defects in a CNT represent sites where chemical bonds may be made and may act as nucleation sites for functionalization agents. The distribution of defects shown in our CNTs (Fig. 12 showing an example with very high defect density) may therefore be to our benefit.

4 Conclusion

The presented method has great potential as a last process step to give nanofunctionality to processed CMOS/MEMS wafers. It is controlled by electrical measurements alone and can thus easily be automated and scaled to wafer level. CNTs

can be used in their virgin state, or they can be functionalized to increase the sensitivity and selectivity to various gases and analytes. Such a system may for instance be used as a sensor for monitoring ageing of food.

The designs presented in this paper show a good uniformity in temperature of the growth structure (variations down to 38 °C). We demonstrate that the simplified two-point resistance measurement corresponds to a good temperature measurement, comparable to the inherently more precise four-point measurement of the central part of the growth structure.

Both ohmic contacts and Schottky junction contacts can be obtained, and very straight CNTs connecting the two microstructures can be manufactured.

The carbon nanotubes produced by the presented method show a large variation in diameter, straightness and degree of order. This is governed by experimental parameters such as local temperature, which necessarily will show a gradient in the growth structures. The CNTs contributing to a closed circuit are the ones guided by the applied electric field during manufacturing. The interaction between CNTs and electric field is shown and explained to be highly diameter-dependent, effectively ensuring that only the thinnest and most straight CNTs are the ones becoming part of a closed circuit. The proposed manufacturing method thus has a built-in sorting mechanism for selecting CNTs with a high degree of order.

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Nanopackaging Requests for Atomic Scale Circuits and Molecule-Machines

Christian Joachim

Abstract Starting from the requirement of fabricating a large atomic flat surface for supporting a functioning electronic atomic scale circuit, the different possible architectures of an atomic scale Boolean logic circuit are discussed in the prospect to be supported by such a surface and encapsulated at the end of the fabrication process. This leads to look after the best possible interconnection strategy to beneficiate from the possibly large calculating power of a large atomic scale circuit. This has many consequences on the final packaging of such a circuit while preserving the atomic scale precision of its construction and while offering a large number of interconnects from the atomic scale to the external world.

1 Introduction

The production of a chip able to take benefit of the quantum (or classical) resources available in atomic scale devices, circuits, and/or molecule-machines (calculators, mechanics) requires the definition of a complete fabrication process from the supporting surface to the nanopackaging end step. On an atomic scale well-defined supporting surface, a few elementary circuits and single molecule-machines have already been constructed and tested using the low-temperature ultra-high vacuum scanning tunneling microscope (LT-UHV-STM) capabilities of imaging and manipulation an adsorbate with a few picometer precision [1]. Mechanical molecular machineries have been molecule-by-molecule LT-UHV-STM assembled and tested like the molecular rack and pinion machinery [2], the single molecule-gear [3], and the single molecule-motors [4]. Mechanical logic gates have

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been molecule-by-molecule constructed using the classical CO molecules mechanical behavior on a metal surface [5]. The first quantum intramolecular logic gates have been tested when the molecule-logic gate is physisorbed on the Au(111) surface [6] and the first atom-by-atom quantum logic circuits has been tested on a Si(100)H surface using STM [7].

After those demonstrations that simple atomic scale machineries can perform a useful function for mechanics and computing operations, it is now time to go a step further. We have to explore how to go from the laboratory LT-UHV-STM surface science experiments mentioned above to a real atom technology able to produce a portable chip where the quantum (semi-classical) behaviors of a few atoms or molecules stabilized on a supporting surface will be used to construct useful and complex nanoscale machines. In the recent years, this direction had already started to be explored with for example the problem of multi-channels planar nano-mechanical and nano-electrical interconnects [8]. Planar mechanical [9] and electrical [10] nano-interconnects have been obtained using diverse nano-fabrication techniques with a special care that the corresponding processes be UHV compatible. Solid-state robust nano-gears have been obtained with the goal to transfer mechanical motion from a molecule-motor to mesoscopic solid-state gear [11]. Solid-state metallic triangle nano-pads have been UHV grown on a specific substrate and then UHV transfer on an Si(100)H surface [12] with prospect to interconnect with atomic scale dangling bond (DB) wire on this surface.

In the following, we propose a systematic overview of all the known steps for the design, the fabrication, and the production of a nanopackaged chip whose functionalities will be based on atomic scale machineries. We restrict ourselves to the prospect of producing electronic calculating machines. As compared to mechanical, there are a few specific constrains to be respected for electronics atomic scale calculating machines like the minimization of the surface tunneling leakage current and the thermal stability. However, many of the process steps described hereafter are generic to both electronics and mechanical atomic scale machines. Section 2 is describing the progresses toward the supporting surface selection and fabrication. Section 3 deals with the possible electronic circuit's architecture and Sect. 4 with the interconnections of this circuit on the supporting surface. Section 5 describes the approach now explored for a nanopackaging of the atomic scale chip like a permanent protection of the atomic scale fabrication precision of the circuit toward any external destructive agents or events. Section 6 is the conclusion of the chapter. It provides a list of problem to be solved for the production of an atomic scale chip to happen.

2 Atomic Scale Surface Preparation

The surface supporting the atomic scale circuit must obviously be fabricated with an atomic scale precision and provide large atomically flat terraces. This is important to have enough space on the surface to develop on the same terrace the atomic scale circuitry and its interconnections. This surface must also have a finite

electronic band gap near its Fermi level for the current intensity passing through the circuit constructed on this surface to be larger in intensity as compared to the through surface leakage current between any couple of metallic nano-pad interconnects. The choice of the supporting surface is also depending on the architecture chosen for the atomic scale electronic circuit. It can be a complex molecule carrying for example all the Boolean logic functionalities, logical inputs, and outputs gates. In this case, the surface is only a passive support. Its atomic scale structure must only be compatible with the positioning of the contacting metallic nano-pads and of the molecule circuits. However, the circuit can also be constructed atom by atom directly on the supporting surface. In this case, the surface over layer will be LT-UHV-STM manipulated atom by atom to obtain the atomic scale circuit by extracting for example hydrogen atoms one by one on the Si(100)H or sulfur atoms on the MoS_2 surfaces [13, 14]. There are also intermediate cases for example a molecule-logic gate may need an intermediate DB wire circuit to be connected to metallic nano-pads and to other molecule-logic gates to form a complex Boolean logic circuit. Another interesting case is a fully conducting surface like graphene where LT-UHV-STM carbon atom-by-atom extraction can lead to atomically well-defined insulating areas and molecular scale circuits with no need to bring on the surface complex molecules.

Considering all those possible cases and depending on the type of circuit architecture, it is important to fabricate a well-ordered surface at the atomic scale supported by a solid whose function is to stabilize the surface mechanically and in some cases to stabilize the interconnections. This surface can exist by itself like a graphene or an MoS_2 single layers or it can exist because of its chemical bonding with an underneath supporting bulk like Si(100)H as it is presented in Fig. 1 or like the AlN(0001) surface. In this second case and from an electronic point of view, the first AlN(0001) surface atomic layer does not define electronically the surface by itself. Native surface reconstruction indicates that the electronic properties of such a surface are also depend on the exact atomic structure a few layer below this surface.

For production as compared to research laboratories, the efforts are now concentrating in the production of large surfaces able to be used in UHV conditions after the fabrication process. There are now well-known cases corresponding to the 3 classes of surfaces described above: graphene (and by extension MoS_2 or TeS_2) monolayers, Si(100)H passivated 2×1 reconstructed surfaces, and for example large gap AlN(0001) robust surfaces. There is no electronic gap for the graphene surface, a 1.8 eV surface gap for an MoS_2 monolayer, and a 2.1 eV surface gap for the Si(100)H surface supported by a bulk whose gap is only 1.1 eV. The AlN(0001) surface is supported by a 6 eV electronic gap AlN bulk material of a thickness of about 100 nm and is usually grown on SiC(100). The exact AlN(0001) surface gap is not known yet.

In terms of wafer lateral size, graphene and MoS_2 monolayer must be supported by an atomically flat underneath surface. For graphene, even ultra-flat SiO_2 surface can create large graphene surface deformation. It is the same for MoS_2. For this case and due to exiting MoS_2 bulk materials (Fig. 2), it may seem more interesting to

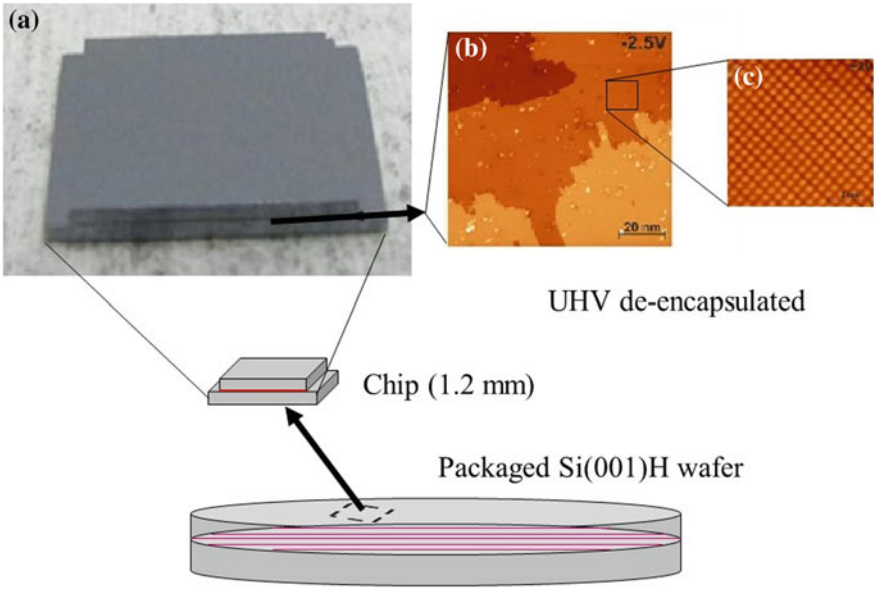

Fig. 1 LT-UHV-STM characterization of a UHV de-bonded Si(100)H surface at 4 K. **a** The 1.2 mm in lateral size chip. **b** Filled state image: −2.5 V, 20 pA (100 nm × 100 nm). **c** Empty states image +2 V, 100 pA (7 nm × 7 nm). Sharp atomic step edges in (**b**) and hydrogen-terminated reconstruction rows in (**c**) are clearly visible. The de-bonded 1.2-mm chip was cut from a 200-mm wafer produced in a clean room [15]

start with a bulk MoS_2 sample and to gently exfoliate a few surface layers to produce at the end an ultra-clean MoS_2 surface van der Walls bonded to its native underneath MoS_2 bulk. But, for both graphene and MoS_2, the problem is the size of the overall samples and their surface quality. They are not yet compatible with a wafer size that can be handled in a wafer fab for wafer preparation and cleaning (compare the Figs. 1 and 2 examples). Ultra-clean graphene monolayer is not extending more than a few 100 μm in lateral dimensions. Comparatively, centimeter scale MoS_2 stones are extracted from mines located for example in Canada or Australia. However, they are usually full of defects and their intrinsic doping is very difficult to guarantee. Nevertheless, MoS_2 wafer can be produced with a few millimeters in lateral size but with many surface steps. Atomic resolution can be obtained and STM atom manipulation performed at the laboratory scale (Fig. 2).

Starting for ultra-flat 200-mm SOI wafers, a complete process has been consolidated recently able to produce a few millimeter in lateral size chips (Fig. 1) where large atomic scale Si(100)H terraces can be found and preserved after going from the wafer fab to the UHV chamber [15]. This is the first example of the production of a wafer compatible with standard clean room equipment illustrating a few essential steps required for the production of atomic scale wafer surface. First, the native initial wafer must be ultra-flat. This seems to be an obvious requirement.

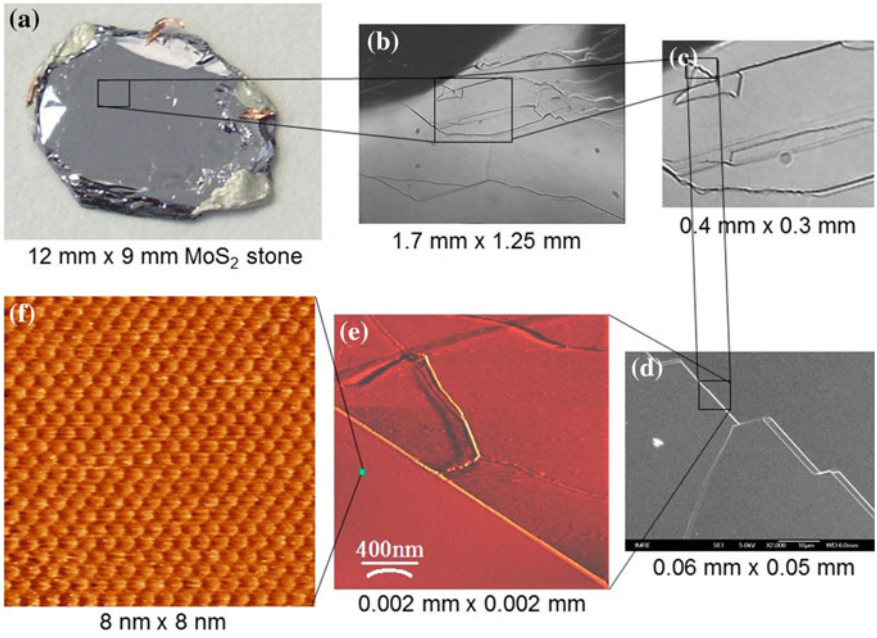

Fig. 2 Example of a bulk MoS_2 "wafer." A 12 mm × 9 mm MoS_2 flat stone was processed from a MoS_2-mined stone and a few top MoS_2 layers were scotch tap exfoliated to get the surface (**a**). This surface is full of steps as imaged using an optical microscope in (**b**) and (**c**). An SEM image (**d**) was used to locate rather flat areas near some step edges. UHV-STM images in (**e**) and (**f**) were obtained to look for atomically flat terraces where atomic manipulation can be performed (STM image: constant current 0.2 nA, 1.0 V)

However, any miss-cut in the definition of the surface orientation will lead to a large series of atomic step on the surface which are very delicate to eliminate even after a few annealing steps. Second, there are a few chemical process steps used to produce the Si(100)H surface [15]. Those chemicals must be selected with care not to induce atomic scale defect on the surface at the end of the process. This is for example the case of Cl precursors. Of course, the annealing temperatures are very important to master to succeed at the end of the process to get large mono-atomic and free of defect large terraces. Notice that we do not know yet the required mono-atomic terrace minimum size and this will certainly depend on the circuit architecture and also on the number of nano-interconnects converging toward this circuit (see Fig. 7). Terraces larger than a few 100 nm in lateral dimension will certainly be required.

Third, the next step in the process flow is the transfer from the wafer fab (generally a class 100 clean room) to the UHV chambers required for the atomic scale construction and interconnects. At the moment, it is not possible to transfer a large 200-mm wafer in one piece due to mechanical stability and also to the

scanning range of an LT-UHV-STM used to construct the circuit. This implies the optimization of a peculiar step in the process flow where the 200-mm wafer must be cut into small chips respecting also the atomic scale cleanness of the resulting chip (see Fig. 1). This is a very delicate step since any cutting process (mechanical, chemical, or ionic) is generating surface reconstruction and edge effect which may propagate through the chip surface. The solution for the production of Si(100)H centimeter size chips is first to cap the full wafer using a wafer bonding process and then to cut this caped wafer in chips and finally to open the chip in the UHV [15]. This is working partially for Si(100)H because such an de-bonding in the UHV seems also to produce atomic scale surface defects.

The production of large electronic gap surfaces like AlN(0001) is natively performed in the UHV using a molecular beam epitaxial chamber. This is suppressing the capping step since all the process from the wafer production to the atomic scale construction will remain in UHV without any UHV breaking along the process flow [8]. Since there is no surface passivation layer known for the AlN (0001) surface, such a large electronic gap surface seems at the moment very useful only for molecule-logic gates. Furthermore, the actual extension of the atomically flat terraces on AlN(0001) is certainly much less than 100 nm which restricts a lot the potential of those surfaces for atom circuit construction. Notice also that atom-by-atom manipulation on a large gap surface requires the development of an LT-UHV non-contact AFM (nc-AFM) technology which is not as mature as compared to the LT-UHV-STM technology of atom manipulations. This also explains why the surface of a true insulator material had not been explored yet for the fabrication of atomic scale circuit.

One has also to consider the influence of the bulk doping in the choice of the bulk material supporting the surface. In the case of an MoS_2 surface supported by the MoS_2 bulk or in the case of an Si(100)H surface supported by its Si bulk, the doping level of the bulk can lead to a considerable electronic band bending effect when for example using metallic nano-pads for fabricating the interconnects on the surface of those materials. This can simply shift the electronics valence and conduction band edges up the surface Fermi level, transforming an insulating surface at low bias voltage in a conductive one. This effect is not yet fully mastered and the best way to avoid this problem is to start with a large surface electronic gap intrinsic semi-conductor bulk material.

Finally, the above-mentioned possible surfaces are coming from standard solid-state technologies taking benefit of a succession of annealing, chemical etching, chemical decomposition of precursors, and rinsing using a lot of different kinds of solvents for the surface preparation. It may be good to explore in the future the production of atomic scale wafers respecting all the criteria described above but fabricated with sustainability for the environment which is not the case actually.

3 Circuit Architecture for the Atomic Scale

Supposing that a wafer with a well-ordered surface at the atomic scale is available to an electronic circuit designer (see for example Fig. 1), what will be its favorite architecture for a calculator machine to be fabricated and then interconnected at the surface of such a wafer? Back to the seminal C.E. Shannon's paper in the late 1930s [16], the now traditional thinking of a calculator structure in real space based on a separation of the circuit in a regularly deposited in space electrical switches (or transistors) is so present that the first temptation for this circuit designer will be to follow this tradition at the atomic scale.

Suppose for now that it is possible to design a 3-terminal device with gain using a single molecule as proposed by Aviram [17] or with a small number of metallic atoms (as proposed by Wada [18]) or of DB obtained for example by extracting surface atoms from a passivated semi-conductor surface like Si(100)H or MoS_2. To preserve the gain per device, each atomic scale transistor (single molecule, atom triode) has to be separated from its neighbor in the circuit. "Separated" means here a true loss of quantum coherence in between each of those active elements along the circuit. This is presented in Fig. 3 where each active device is surrounded by "decoherers." Those decoherers can be for example long enough metallic nano-pads to pass from the molecule itself to the metallic interconnection wires. They play the essential role of making the quantum phase of each transferred electron through the active molecule to be lost. In such a way and from the wiring, such molecular device can be characterized by a standard I–V characteristic depending of the grid voltage like any 3-terminal device. The disadvantage of this approach is that those decoherers are taking a lot of space in the circuit design. This is the explanation why quite early in the history of molecular electronic, researchers such as Carter [19] have proposed in 1984 to miniaturize the total circuit inside a very molecule as presented schematically in Fig. 4 suppressing all those decoherers-like devices inside the circuit itself.

This leads to some proposals of very complex and unrealistic mono-molecular circuits [20] after supposing that the G. Kirchhoff electrical meshes and node circuit laws were valid at the atomic scale, which is wrong for molecules and also for atomic scale circuits constructed atom by atom on a surface [21].

But rather than keeping the topology of real space circuits with switches, transistor, meshes, nodes, and wires inside a single molecule, another possibility is to manipulate quantum information with or without exchanging electrons between the different parts of an extended quantum system. For performing a calculation, and when the quantum system is prepared in a non-stationary initial state, why not using its spontaneous time-dependent response before the quantum system is relaxing in its ground state.

In our days, the most popular way of designing a quantum computer is to separate the quantum system in the so-called qubits as it was proposed by Feynman [22] in the mid-1980s.

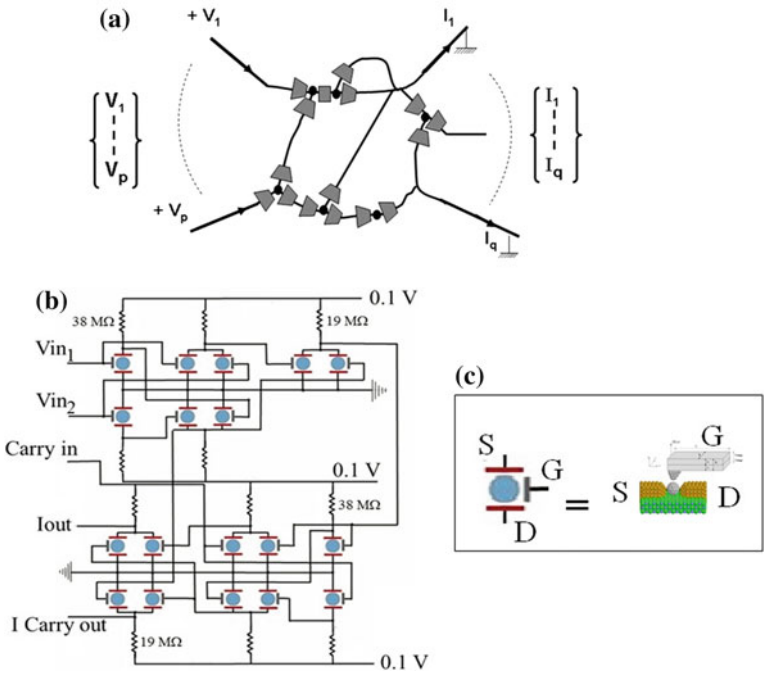

Fig. 3 **a** The well-known setup of a hybrid molecular electronics circuit where all the active elements (figured here by a *black dot*) have been isolated from each other's by "decoherers" and then interconnects by classical non-ballistic wiring. This is represented here by inserting as many as required classical to quantum (C/Q) and Q/C convertors along the circuit represented by the *gray trapezoidal blocks* in (**a**) (two to three per active devices). The information input is encoded in the $\{V_1, \ldots, V_p\}$ classical voltage word and the output in the $\{I_1,\ldots, I_q\}$ current intensity word. **b** The example of an hybrid digital 2 digits full adder with its carry in and its carry out designed following this hybrid architecture. Each *blue large dot* in (**b**) is a single C60 transistor represented in (**c**). There are 18 single molecule transistors in this circuit all interconnected by classical electrical wires. Each *blue dot* is corresponding to a *black dot* of the schematic diagram (**a**) (see [46] for more details). A SRAM circuit had also been designed with a specific packaging [23]

A qubit is a 2-level quantum system which can be prepared in a normalized superposition of 2 quantum states following the principle of quantum superposition. A N-qubits quantum system can be maintained in interaction using for example the skeleton of a molecule. Starting from a well-prepared N-qubits non-stationary state, the time-dependent quantum evolution of this N-qubit system can be represented on the quantum states space (isomorphic to the Riemann Hypersphere).

Some parts of the surface of this hypersphere are corresponding to the results of the computation. By programming a peculiar time sequence of operations to maintain the N-qubits trajectory on track, the computation must be performed before the N-qubits relaxes in its ground state. This sequence of operations is called a time circuit. Notice that there is no exchange of electrons during such a process, based only on the manipulation of the interaction between the N-qubits. Therefore,

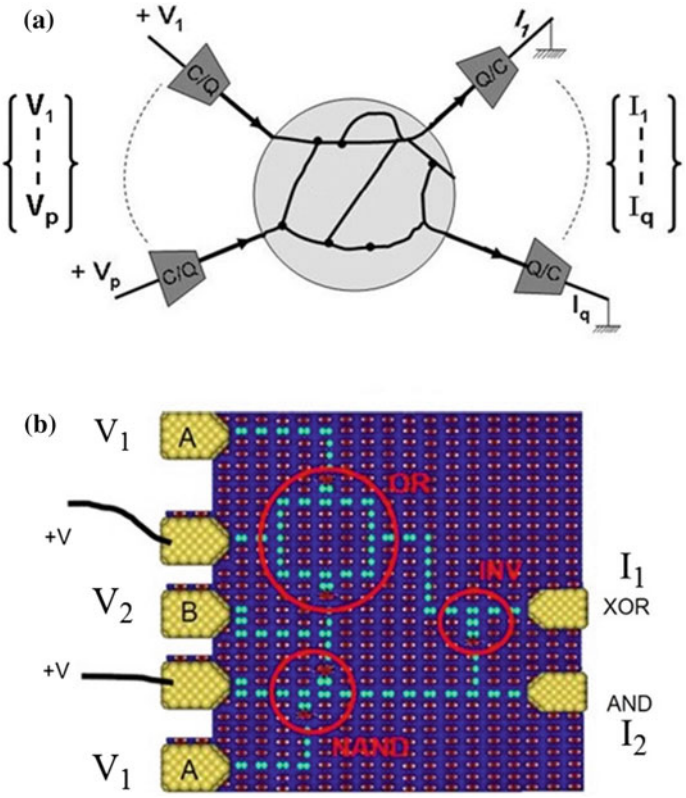

Fig. 4 **a** The semi-classical-integrated circuit version of Fig. 3 classical electrical setup where the circuit inside the molecule still looks like a classical electrical circuit with nodes, meshes, and active intramolecular chemical groups (the *black dots*) but all intrinsic to the molecule. The input and output information encoding is the same than in Fig. 3. Well-adapted semi-classical circuit rules have to be applied to design intramolecular circuits or dangling bond circuits where the C/Q and Q/C convertors are metallic nano-pads external to the circuit itself. **b** A top view of an atomic scale circuit digital ½ adder supposed to be constructed atom by atom on an Si(100)H surface whose lateral size is 36 × 20 Si dimers. This circuit was designed following the standard classical electrical circuit for a Boolean ½ adder supposing also that the cascading between 2 gates (for example between the NAND and the Invertor) is possible without any decohence process

the approach is orthogonal to the previous mono-molecular real space circuit one presented in Fig. 4 where billions of electrons transfer per second were supposed to be occurring between each part of the circuit.

In between the real space circuit design proposed in Fig. 4 and the qubit approach described in Fig. 5, it exists an intermediate new approach called the quantum Hamiltonian computing approach (QHC) [23]. Here, the spontaneous quantum evolution of a quantum system prepared in a non-stationary state is also used and the Hamiltonian of the quantum system is still the generator of this evolution. But in QHC, the logical input information is inputted directly on the Hamiltonian and not in the initial quantum state vector.

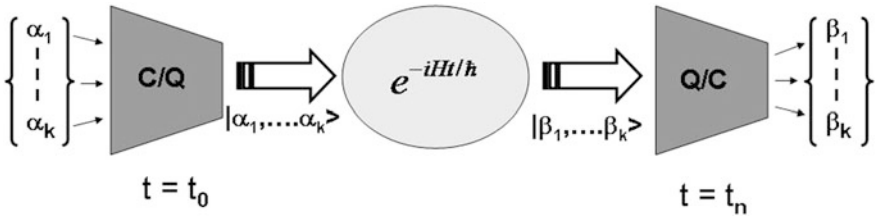

Fig. 5 The formal setup of a quantum computing system where the central gray quantum system can be an organometallic molecule with its qubits distributed along the molecular skeleton (not represented) or single atomic impurities embedded in a semi-conductor solid matrix. The $\{\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\}$ classical digital inputs are converted into quantum information by the C/Q convertor in charge of preparing at $t = t_0$ the initial quantum state vector $|\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\rangle$. For $t > 0$ and at each time $t = t_n$, the $|\beta_1, \ldots, \beta_i, \ldots, \beta_{k'}\rangle$ output quantum state vector is reached and measured using the quantum to classical Q/C convertor generally a projective multi-channel measurement system [24]

As a consequence, a given $\{\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\}$ classical digital input word on the Hamiltonian, i.e., $H = H(\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k)$ is controlling the quantum trajectory of the QHC system. The output can be measured by awaiting on the quantum state space for the quantum trajectory to reach the awaited quantum target state $|\beta_1, \ldots, \beta_i, \ldots, \beta_{k'}\rangle$ leading to $\{\beta_1, \ldots, \beta_i, \ldots, \beta_{k'}\}$ by a Q/C conversion or by measuring the secular oscillation frequency ω_{dp} of the corresponding time evolution between the given initial $|\psi_d\rangle$ and target $|\phi_p\rangle$ states. Quantum states $|\psi_d\rangle$ and $|\phi_p\rangle$ are always the same for all the input and output logic configurations. They do not carry any direct logic information. In QHC, a very fast oscillation encodes for a "1" and a very slow oscillation for a "0" logical outputs. A symbolic analysis of the QHC approach has been demonstrated which relates a given ω_{dp} to a given $\{\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\}$ digital input word [25].

The quantum time evolution $|\psi(t)\rangle = \mathrm{e}^{-\mathrm{i}Ht/\hbar}|\psi(0)\rangle$ is controlled by oscillation frequencies whose values are simply the two-by-two differences of the $H(\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k)$ eigenvalues. As a consequence, changing H using the $\{\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\}$ input words is modifying the H eigenvalues and therefore the ω_{dp} secular frequencies. Interestingly, a very attractive way for the atomic scale planar implementation of QHC is the fact that the current intensity between $|\psi_d\rangle$ and $|\phi_p\rangle$ is proportional to the square of the ω_{dp} Heisenberg–Rabi oscillations occurring between $|\psi_d\rangle$ and $|\phi_p\rangle$. As presented in Fig. 6, this leads to a very elegant formal architecture of a QHC calculating system where the output word is simply the different current intensities corresponding to the different Heisenberg–Rabi time-dependant evolution processes required to construct the digital logic output word. Notice that the $\{\alpha_1, \ldots, \alpha_i, \ldots, \alpha_k\}$ input words are classical words that are converted into quantum information available on the system since the H eigenvectors are changing each time a new input word is entered on H. All the 2 inputs–1 output digital logic gates Hamiltonians have been constructed this way [26]. From the eigenstates symmetry of those Hamiltonians, simple π system

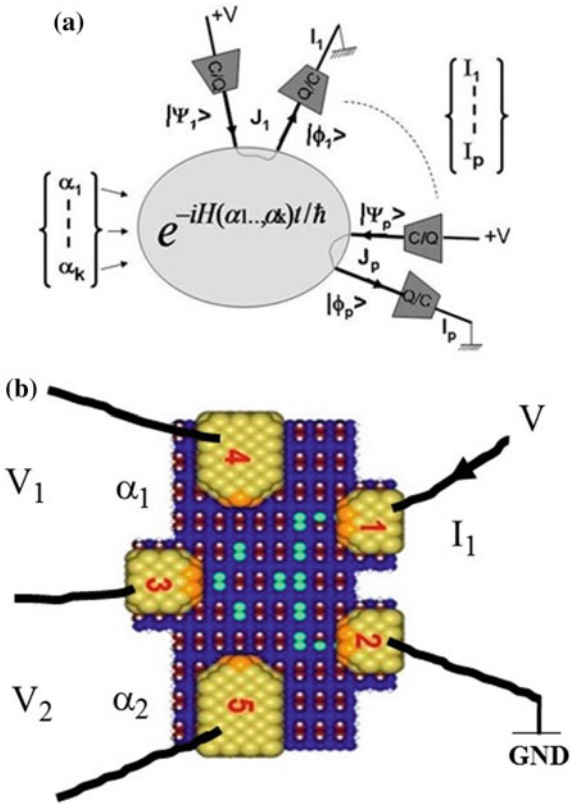

Fig. 6 **a** The formal QHC approach with its classical inputs on the quantum Hamiltonian of the system and the local current outputs $\{J_1, \ldots, J_p\}$ in charge of measuring the logical output Heisenberg–Rabi oscillations. **b** A practical dangling bond surface implementation of a QHC AND on a Si(100)H surface. The logical output current is measured between the Au nano-pads 1 and 2 while the 2 logical inputs are inputted using the two small voltages V_1 and V_2 triggering through the input dangling bonds an inelastic current effect able to switch a molecule-latch (not represented)

topological Hückel matrices were established and enlarged respecting symmetries and the spatial position where to read the output on the quantum system. The chemical structure of the QHC starphene NOR gate molecule was determined following this procedure [27] and Fig. 6b Si(100)H surface dangling circuit was designed also following a QHC approach starting from a very simple tight-binding quantum graph [28].

As described in this section, there are four different possible calculator architectures that can be implemented at the surface of a solid: hybrid architectures with a classical electrical wiring in between each active device (Fig. 3), monolithic architectures with still a semi-classical design of the circuit inside the molecule or the DB circuit (Fig. 4), the qubit approach where each qubit must be spatially separated from the others to avoid any electron transfer processes (Fig. 5), and

finally, the QHC approach which do not require the separation of the calculating quantum system in qubits (Fig. 6). Among those, some architectures are more appropriate in terms of surface interconnects and as a consequence in terms of packaging. This will be discussed in the next 2 sections.

4 Interconnects

As illustrated in the previous section, the integration of a large calculating function with single molecule(s) or at the surface of a semi-conductor (for example) using a DB atomic scale circuit necessarily requires many electrical wires converging toward and coming from the atomic scale. This is for example the case of Fig. 4 DB circuits where 5 metallic nano-pads have been employed in a semi-classical like design even if this circuit is only performing a simple XOR Boolean logic function.

The power law describing the increase of the number of interconnects as a function of the calculating power of a machine is a well-known problem in technology. For atomic scale circuits, it raises at least 3 questions: (1) how to minimize the number of atomic scale interconnects between the different active element of a complex atomic scale circuit, (2) how to pass from the quantum local behavior of the atomic scale circuit to the nanoscale metallic electrodes supposed to drive and extract some electronic currents and if necessary to apply some bias voltage, and (3) what is the fabrication technology to pass from the nanoscale to the micron scale where standard micro-electronic technologies can be applied. In this section, we will discuss the first 2 questions. The nano- to micro-passage will be discussed in the next Sect. 5 devoted to nanopackaging because packaging and nano- to micro-interconnect are directly related.

Starting by question 1, at the surface of an atomically precisely fabricated chip and considering an atomic scale circuit of diameter D, how many metallic nano-interconnects N are required to converge toward the same nano-spot of diameter D on the surface as a function of the atomic wire width δ and for a given inter-atomic wire distance d at the interconnection point as presented in Fig. 7?

The simple geometric answer to this question is

$$N = \pi D(d + \delta)^{-1}$$

Using atomic scale wires for surface interconnects, with a section of a single atom, the minimum value for δ is simply twice the van der Waals radius of the corresponding atom. For surface DB wires, it is simply the effective molecular orbital lateral expansion of the corresponding DB in the surface that is about $\delta > 1$ nm. For metal atom, the construction of long atomic wires will result from STM atom-by-atom lateral manipulations on a surface which will guarantee that their individual adsorption site is able to fight against metallic cohesion [29]. Surface DB wires will result from STM vertical atom manipulations extracting one-by-one surface atoms to free a set of atomic orbitals per surface atom [30]. Supposing that

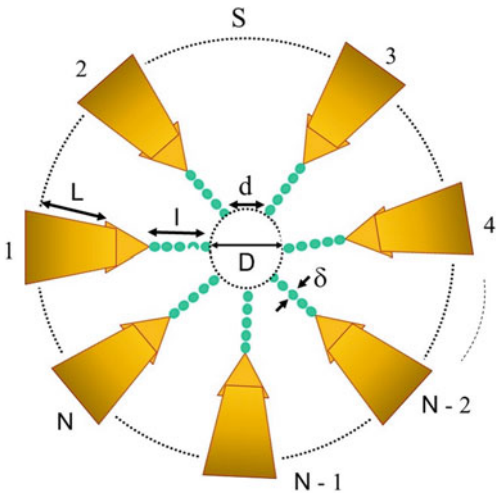

Fig. 7 A schematic representation of an N nano-electrodes planar device for the electronic interconnection of a central atomic scale circuit of effective diameter D. The atomic scale wires of section δ are positioned around the central circuit with an inter-wire distance d. In charge of the interconnection to the mesoscopic and the macroscopic scales, metallic wires are starting at a distance $L + T + l + D/2$ from the center of the circuit which defines a circle of diameter S. T is the lateral size of the triangle metallic nano-pads in charge of converting the electrons transfer processes in an average electronic current flow through the device. Each atomic scale wire of length l can be a dangling bond wire, a single-wall carbon nanotube, or a molecular wire

very long atomic wires can be STM constructed atom by atom, the limit on N for a given D is imposed by the surface leakage tunneling current in between 2 such wires that can be tolerated for the atomic or molecular circuits to be functioning.

Taking a standard large gap insulating surface for supporting the atomic scale circuit of diameter D, an acceptable leakage current intensity lower than a few fA leads to $d > 1$ nm at the interconnection side between the atomic scale circuit and the atomic wires for a bias voltage of about a volt. For a low gap semi-conductor surface, the fA leakage current regime will be reached for $d > 10$ nm and for a much lower bias voltage.

Those numbers are putting an extreme constrain on the size of the atomic scale circuit which would be accessible using N contacting nano-pads. For a very complex and large calculating molecule of an effective lateral size of about $D = 5$ nm, this will lead to $N < 10$ on an insulator and $N < 2$ on a semi-conductor surface which is not possible. As a consequence, the number N of required interconnects is very limited by the electronic characteristics of the supporting surface and care must be taken to optimize the calculating power of an atomic scale circuit given its lateral extension D.

This limitation has a very challenging consequence for atomic scale circuit design and packaging. According to the above Sect. 3, they are few possible circuit architectures at the atomic scale. For a standard circuit design based on the

Kirchhoff's laws and aside from the fabrication and the physical limits on δ and d, there is also a practical limit on N for a given D. Already for micro-electronics, due to the Kirchhoff's laws and for an interconnected circuit of M transistors, the empirical relation $N > k\,M^p$ ($k = 2.24$ and $p = 0.5$) limits the number of interconnects required in average by a designer to interconnect a complex logic circuit [31].

For the atomic scale, if the diameter D of the calculating molecule is too small, there will be of course not enough space in the molecule or in the atomic circuit to support, in a classical circuit design meaning, a given calculating power (measured for example by the complexity of the logic gate performed by the molecule circuit). In this case, a complex logic circuit will require a very large molecule, may be in the $D = 10$ nm range and the number N of required interconnects will be rather limited. On the contrary, if a large calculating power can be implanted in a molecule for example by a quantum approach as discussed in Sect. 3, difficulties will arise since it will be impossible to effectively construct N enough atomic wires converging toward this molecule to benefit from its large calculating power. This will force the designers to compromise between the calculating power of a given elementary quantum circuits and the number of such quantum circuit to be interconnected semi-classically together to reach the maximum possible calculating power. It is here important to notice that we do not know yet the maximum calculating power reachable for example by a single QHC atomic scale circuit before losing its quantum coherence. Boolean "2 inputs–1 output" logic functions have already been demonstrated experimentally as discussed in Sect. 3. A Boolean "2 inputs–2 outputs" ½ adder logic function has been designed at the atomic scale. It is not known if larger QHC Boolean logic functions can be designed for example a Boolean 2×2 full adder (or more).

When the elementary functional building blocks of a complex calculating circuit are transistors, the interconnection strategy is to play with the empirical relation $N > k\,M^p$. For a more complex elementary building block like a QHC logic function, what would be the building block to be considered instead of the transistor and to be counted by M? It may come out that a regular network (a circuit) of this new and more complex QHC building block be not very efficient as compared to a network of transistors. In that case, emerging semi-classical behaviors of a random network of those QHC building blocks as for example proposed with classical random networks of switches [32] will do the job which will ease the nano-construction and the nano-interconnects arrangements. It may also turns out that due to this interconnection problem (the tyranny of numbers as it was called in the 1950s before the invention of the monolithic integrated circuit concept), only elementary blocks functioning like transistors will be used.

For question 2, it is important to insist on the dual role of the metallic nano-pads located in between the atomic scale wires of section δ and the micron scale interconnects and represented in Fig. 7 by triangles of lateral size T. Those nano-pads are required to physically and continuously pass from the nanoscale to micron scale using the same type of materials in an adiabatic-like transition. For this purpose, the material can be a noble metal or a piece of metallic graphene. But as already notice in the previous section, those nano-pads are also required to convert the billions of

quantum electron transfer events per second occurring along the atomic scale circuit in a measurable electronic current flow [33]. This second function is not often recognized since the discussion is always oriented toward metallic electrode adiabatic size reduction from the micron scale toward the nanoscale.

This conversion is a very important effect where it is generally more efficient to use in fabricating the nano-pads a material with a large and stable density of electronic states at Fermi level. This will ensure a large efficiency of this conversion. This is certainly the case for nano-pads made of non-magnetic noble metals. But, this is more problematic for a single sheet of graphene whose lateral size is to be reduced step by step from the micron down to the nanoscale. The existence of this quantum to classical conversion physical process (or the reverse classical to quantum conversion) leads to a net difference between Ohmic (or Schottky) contacts and atomic orbital to atomic orbital hybridization at the atomic scale contact. When the end of an atomic scale circuit is in electronic interaction with the end atoms of a metallic nano-pad, an electronic contact can be also well-defined and optimized considering that: (1) When a covalent bond is formed in between the two (about 0.22 nm in distance), the local density of states of the metallic nano-pads is modified by this bonding and the contact resistance is large; (2) when the inter-atomic distance between the two is larger than the van der Waals distance, the contact resistance is very large; and (3) in between the two, there is an optimum distance about 0.26–0.29 nm to get a good contact resistance for a conjugated molecular wire whose end is in a coplanar interactions with the surface end of the metallic nano-pads [34]. This is not a Schottky contact and the concept of Ohmic contact cannot be applied in this context.

As presented in Fig. 8 and Fig. 7, metallic triangle nano-pads can be deposited first on the atomically flat and ordered supporting surface and this well before the atomic scale manipulation required to construct the interconnection atomic wires of section δ (see also Fig. 10). Then, the supporting surface has to be cleaned atomically again and the atom and molecule manipulations performed at the end of this cleaning step. There are two main problems with this approach: Standard UHV cleaning procedures are so destructive, using for example high temperature annealing and successive steps of sputtering that the interconnection metallic nano-structures will not survive this cleaning. Secondly, STM atom and molecule manipulations are requiring exclusive atomically flat surface areas for the lateral facets of the tip not to interact with the edge of those triangle nano-pads during the STM manipulation steps. These constraints would impose to bury the contacting metallic nanowires into the surface. This had been achieved earlier with nanoscale precision [35], but certainly not with atomic scale precision.

In another approach, the surface is first prepared using UHV surface preparation techniques leading to very large and atomically flat terraces. Then, the atom and molecule manipulations will be performed to construct the interconnection surface atomic wires and to position the molecule circuit in the center of this nanoscale interconnection structure. The nano-electrodes network would be fabricated at the end of the process flow using for example the UHV compatible nano-stencil technique [36]. The problem is that no atomically, STM constructed nanostructure

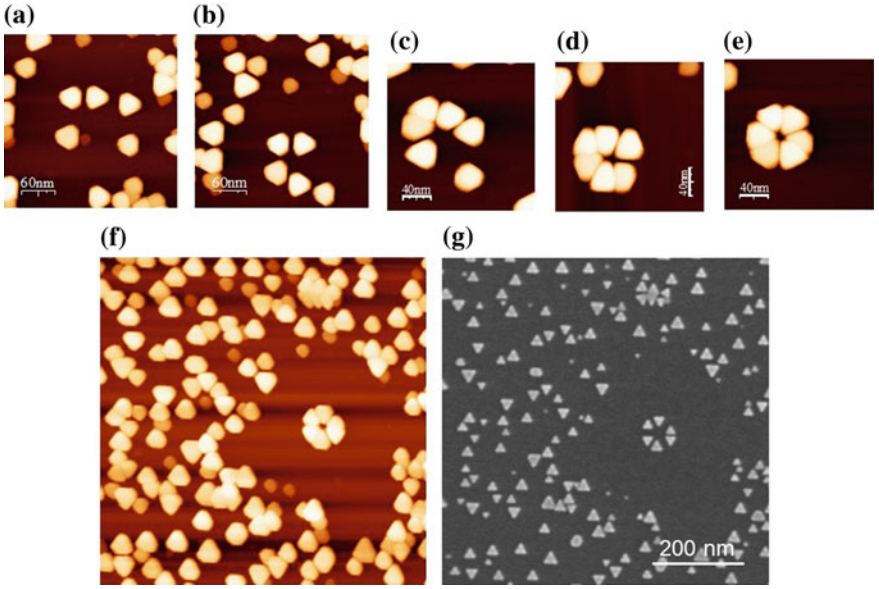

Fig. 8 An example of the construction of a 6 metallic nano-pads interconnects on an MoS_2 surface. After the growth of 30 nm in lateral size triangle nano-pads (10 nm in thickness and well 111 facetted), each nano-pad is UHV-STM manipulated. The manipulation sequence from (**a**) to (**e**) is a short summary of the multiple manipulation steps which have been required to pass from (**a**) to (**e**). At the end of the STM manipulation, a large UHV-STM image (**f**) is compared with the same area UHV-SEM image to appreciate the real inter nano-pads distances. *Scale bar* for **a**, **b**: 60 nm, for **c**–**e**: 40 nm, and **f**, **g**: 200 nm. In the center of the 6 nano-pads structure in (**e**), the diameter D defined in Fig. 7 is $D = 20$ nm. STM image scale bar from **a**–**f**: 15 nm from *white-yellow* to *dark orange* (see Ref. [10] for more details)

can withstand standard nanofabrication techniques nor the surrounding metallic deposition imposed by this nano-stencil technique. For example, the use of wet (dry) etching steps along the process flow would destroy the atomically constructed nanostructures. At this stage, it becomes now important to discuss the packaging procedure to learn how nanopackaging can help in solving this interconnection problem.

5 Nanopackaging

Packaging and "nanoscale to micron scale (and more)" interconnection technologies are closely related since going out of the nanoscale toward the macroscopic world (or the reverse) necessary requires some physical support to hold the multiple electrical interconnection nanowires located somewhere around the atomic scale chip as presented in Fig. 7. The packaging of an atomic scale circuit chip is also very important to master since the delicate atomic scale arrangement of the circuit

itself needs to be protected from the ambiance atmosphere and from any mechanical destruction.

For a total protection of the chip, a straightforward solution is to grow directly on top of the atomic scale circuit a protective over layer. This solution was already implemented by M. Simmons and its group by epitaxial growing a semi-conductor material on top of an atomic scale STM constructed circuit [37]. For this circuit, it turns out to be a very efficient packaging solution since this growth not only protects the circuit from the environment but also stabilizes its electronic function by bringing the required number of conducting channels to the surface P-doped nanowires [37]. This points out that any layer deposition (thermal, sputtering, and epitaxial) will bring on the atomic scale circuit surface enough chemical materials to certainly transform the atomic scale arrangement of this circuit. This can be beneficial in certain specific cases but not in general.

The same problem occurs when envisaging to deposit, grow, or sputter the metallic nano-electrodes for the nano- to micron interconnection passage directly on top of the atomic scale circuit. This will inevitably require some protecting layer to avoid for example large surface leakage current intensity due to the necessary step-by-step increase of the lateral size of an interconnect for the nano- to the micron size (and more). This demonstrates that packaging and nano- to micron (and more) interconnects are in intimacy.

To establish a large number of electrical interconnects from the nano- to micron scale, a fully planar multi-contact interconnection configuration seems necessary. But, the fabrication of such a complex interconnection network atop of the atomic scale circuit will be very destructive for the circuit itself while using the known nanofabrication techniques. For example, e-beam nanolithography and nano-imprint techniques are using layers or resists which will immediately contaminate the atomic scale surface circuit, rendering atomically precise interconnects impossible. Using e-beam lithography, 2-nm inter-electrode distances have been obtained in a two-terminal coplanar junction configuration [38]. But those junctions have no definite and reproducible atomic scale structures. Furthermore, for more than two electrodes, the back-scattering electron effects with e-beam lead to much larger inter-electrode distances and gaps [39]. This is well presented in Fig. 9 where a maximum of 20 metallic nanowires have been nanofabricated using e-beam nanolithography following Fig. 7 design concept. Thus, atomic scale planar interconnection nano-structures are not possible by this method. Nano-patterning by the nano-stencil technique avoids the problem of surface contamination by resist, but is not an atomically precise fabrication technique. It is not able to define a multi-electrode atomic scale interconnection nanostructure because the metal atoms are diffusing on the surface beside the masked areas causing lateral contamination, and no atomic wires can be fabricated this way [40, 41].

The apparent incompatibility between the atomic scale and the nano-fabrication steps to be performed in sequence at the same surface of a wafer to interconnect an atomic scale circuit to many nano-pads up to the micron scale (and more) leads us to propose an integrated process flow where the two apparently incompatible scales are separated using an SOI wafer: the atomic scale preparation and manipulation

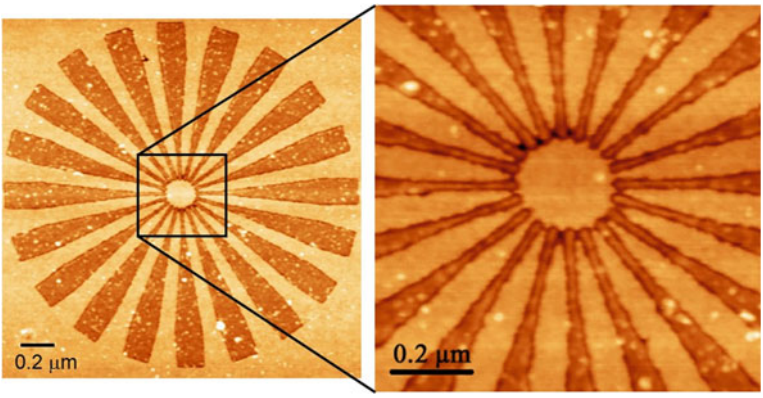

Fig. 9 The AFM image in contact mode of 20 metallic nano-interconnects e-beam lithographed and converging toward a diameter D = 200 nm SiO_2 ultra-flat area. Respecting part of Fig. 7 design, each AuPd metallic electrode is δ = 20 nm wide in the center and 200 nm wide at the other side. Each electrode is buried by 3.5 nm down the SiO_2 surface (the difference between *deep* and *light orange* AFM corrugation. Notice the difficulties to maintain non-contacting electrodes at the center of this interconnection structure (see Ref. [47] for more details)

techniques on the SOI side of the wafer and all the other steps from the nano- to the micron scale on the other side of the same wafer [42]. Such a separation is well known for micro-fabricated sensors where the electronic part of the sensor has to be separated from the often aggressive sensor environment at the front of the wafer [43].

In our case, the passage figured out in Fig. 10e from the back to the front sides of the wafer must be nano-fabricated and not micro-fabricated. As demonstrated in [42], the passage from the back to the top side of the wafer can be obtained on an SOI wafer by etching the wafer from the back to the front. The etching is stopped just before an atomic scale deformation of the front side surface occurs. In this process flow, the atomic surface preparation step is supposed to have been performed first, using standard UHV surface preparation techniques and UHV-STM atomic scale characterization Fig. 10a. To get an atomically flat and well-structured surface on SOI, the preparation conditions are now well-known [44] and enter in Sect. 2 discussion. Then, this surface is encapsulated to protect the atomic scale surface quality from further standard nano- and micro-fabrication steps of our process flow [42]. The demand here is that all the successive process steps after this first surface preparation will be compatible with the thermal stability of the SOI atomic scale prepared surface. This requires a nice thermal budget balance, a balance which remains to be studied in detail.

The consequence of Fig. 10 process flow is that the encapsulation step initially introduced to protect the atomic scale circuit side during the backside of the chip wet process can also be used after to finally nanopackage the atomic scale circuit itself by performing another wafer bonding step in the UHV chamber. It remains

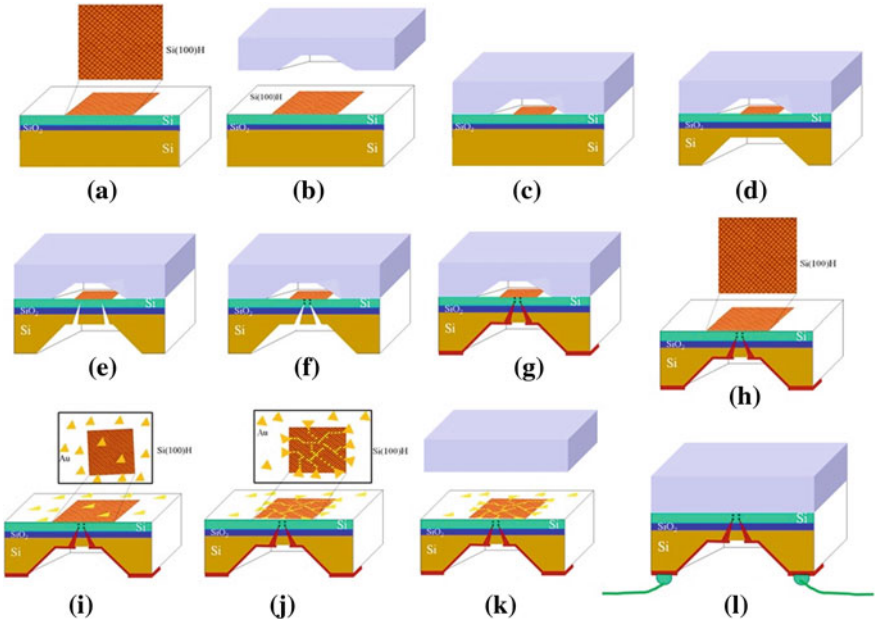

Fig. 10 A complete process flow for fabrication a full packaged atomic scale chip. The process starts with the preparation of a 200-mm SOI wafer whose surface is Si(100)H terminated on large terraces [15]. Chips a few centimeters in lateral size are diced from this wafer leading to the starting step **a** of the figure. **b** After LT-STM UHV inspection of the atomic scale surface quality, this chip is encapsulated again but with a large cavity in the cap not to destroyed the Si(100)H surface. **c** The encapsulation is sealed hermetically to avoid any further opening up to step (*8*). **d** A large 50 µm in lateral dimension backside opening is obtained up to the SOI back surface. **e** FIB piercing is practiced from the back to path through the oxide and stop just before reaching the Si (100)H top surface. **f** As or B dopant are implanted by diffusion through the corresponding holes and activated. **g** FIB is again used to fill up the nano-via with metal. **h** After the microlithography is completed by standard e-beam lithography, the protecting cap is open and the atomic scale surface trouble checked again. **i** UHV transfer print metallic nano-pads are softly UHV transfer printed on the Si(100)H surface [12]. **j** After UHV-STM manipulating those metallic nano-pads laterally to free a large Si(100)H surface, the dangling bond (DB) circuit and its atomic scale wires interconnects are constructed atom by atom by UHV-STM vertical manipulation. The required metallic nano-pads are manipulated in such a way to interact electronically with the DB wires' end and to overlap with the backside-doped area. This is the delicate alignment step between the top and the backside of the chip, facilitated by the STM imaging of the dopant localization from the top side. **k** After a final UHV-STM imaging and if necessary a UHV-4 STM characterization step to certify the atomic scale connections from the top and the top-backside electronic continuity, the chip is nanopackaged again. **l** Micro-wirings are performed from the backside of the chip. Notice that some intermediate step in this process flow has been omitted for clarity (see for example Chap. 6 of this volume)

here to determine the residual gas pressure required inside this nanopackaging cavity and if a rare gas needs to be introduced inside after the wafer bonding step to stabilize the atomic scale circuit further.

6 Conclusion

We have described the possible steps of the design, the fabrication and the production of a nanopackaged chip whose functions will use atomic scale machineries. In this process flow, the first important step is the preparation of a large atomic scale surface able to support the construction of an atomic scale circuit. For this first essential step, at lot of problems are still existing like the ultimate size of the atomically flat terraces that can be produced or the much reduced choice of available surfaces. We are still balancing here between traditional solid-state-based materials such as Si, Ge, or binary semi-conductor compounds and "modern" 2D materials such as graphene or MoS_2. To be constructed and packaged at the surface of one of those materials, four different possible atomic scale circuit architectures were briefly described starting from the standard hybrid molecular electronic approach toward the more actual quantum architectures with or without qubits. Molecular circuits and molecule circuits (semi-classical or quantum) are now in balance with their DB semi-conductor surface equivalents. Classical and quantum circuits can also be constructed atom by atom. At present, it may appear to be very slow to construct such a circuit using the STM single-atom manipulation technology calling from a speed up of the technology. Here, the apparent advantage of synthetic chemistry in terms of throughput is counterbalanced by the difficulties to bring and manipulate a single and large molecule on a surface at the good place with an atomic scale precision. May be on-surface chemistry and self-assembly can be of some help in this case [45]. The raising complexity of multiple interconnections was discussed with the required balance between complexity and accessibility and this whatever the architecture which will be selected for the atomic scale calculator with the care that there will be certainly too much calculating power in a single large molecule to be accessible from the external world. Furthermore, we have not discussed about the frequency bandwidth of those interconnects. The RC constant of each of those may be not so small which will limit the response access time to and from the atomic scale circuits. A simple calculation immediately shows that for a few pico-farads of stray capacitance per interconnect and a minimum nano-interconnect wire resistance around 12 kΩ (one channel of conductance), the maximum bandwidth for exchanging information with the atomic scale circuit will be limited to 100 MHz. A complete nanopackaged process flow was finally suggested with 12 principal steps (not including all the intermediate technical steps). It results that a full nanopackaged chip based on an atomic scale circuit will required a very precise thermal budget to preserve the atomic scale circuit but also its interconnects. This is a formidable (but attractive) technology challenge.

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Single-Crystal Au Triangles as Reconfigurable Contacts for Atomically Smooth Surfaces: Ultra-High Vacuum Transfer-Printing

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Abstract In a planar atomic-scale device, defined nano-contacts to liaise between the atomic scale and the macroscale via the intermediate micron scale are crucial to ensure the atomic-scale circuit performances by minimizing the leakage current, minimizing cross talks, and minimizing contact resistance. Whether the macroscale contact is via a multi-probe system or via doped back interconnects preparing for a nano-packaging, defined and easily recognizable contact nano-pads are necessary. A new approach is presented here based on the in situ transfer of single Au crystals grown on a MoS_2 surface in ultra-high vacuum (UHV) onto another surface where such metallic nano-crystal growth is usually not compatible. The molybdenite surface is particularly well suited to grow single Au nano-crystal triangles, and transfer-printing in ambient environment has already been successfully demonstrated. A dedicated transfer-printing tool was designed and constructed to perform this transfer printing task in a UHV environment. Preliminary results from scanning electron microscopy and low-temperature scanning tunneling microscopy are presented.

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1 Introduction

Nano-imprint, Nano-stencil, or e-beam nano-lithography techniques are not atomic scale in fabrication precision. They are also very damaging to the underneath supporting surface, which can be critical when atomically smooth surfaces are needed for further atomic-scale constructions, fabrications, and processing. In the context of the AtMol (Atomic Scale and Single Molecule Logic Gate Technologies) FET-ICT integrate European project [1], we have developed an ultra-high vacuum (UHV)-compatible nanotechnology able to bring metallic nano-contacts on top an atomically well-prepared semiconductor surface. The AtMol consortium is working on a comprehensive process flow for the construction of a molecular chip, i.e., a molecular processing unit comprising single molecule(s) of surface circuitries connected to external mesoscopic electrodes by atomic-scale precision constructed dangling bond wires or single molecular wires. The integrity of the atomic scale constructed logic gates and circuitries is therefore relying on an atomically clean surface. Hence, it was necessary to develop new planar nano-interconnection techniques that are free of any masking procedure to pass from the atomic scale to the mesoscopic scale and so on. Here, we present a new type of transfer where grown crystalline metallic nano-pads are transferred from an ultraclean stamp to a passivated semiconductor surface in a UHV environment.

2 Ultra-High Vacuum-Compatible Transfer-Printer

The UHV system hosting our UHV transfer-printer has already been described in details in a previous publication [2], as well as in the first volume of this Springer book series [3]. In summary, four independently controlled UHV scanning tunneling microscope (STM) tips under a scanning electron microscope (GEMINI column) constitute the heart of our multi-probe system as shown in Fig. 1. These combined facilities allow macro- to nanoscale and nanometer scale imaging in situ. The multi-probe chamber itself is attached to a low-temperature UHV-STM (with a low-temperature sample transfers between the two, down to 30 K), and a UHV preparation chamber. To this last chamber, another chamber is attached, hosting our UHV transfer-printer (numbered 5 in Fig. 1).

In a previous publication [4], the principle of an Au nano-island transfer-printing technique has already been demonstrated in air starting from stamps and sample prepared in a clean room environment. Since the Au metallic nano-islands cannot be grown crystalline directly on a hydrogen passivated Si(100) 2 × 1 surface without destroying the atomic structural order of this surface, a process was previously optimized to grow first triangular Au single-crystal nano-islands with a lateral size between 20 and 50 nm on an MoS_2 surface. Those nano-islands were subsequently transfer-printed on a hydrogen silicon surface in a class 1000 clean room environment. Unfortunately, the atomic-scale quality of an Si(100)2 × 1H

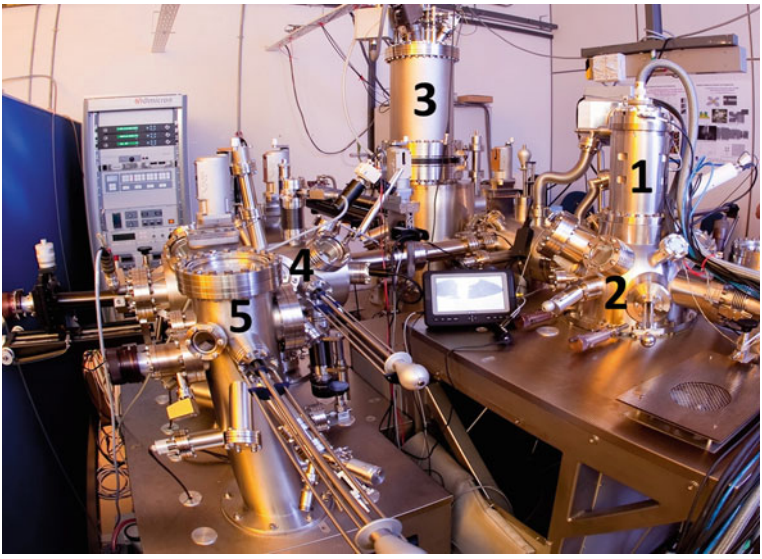

Fig. 1 Photography of the IMRE Singapore multi-probes system comprising a UHV-SEM (*1*), the multi-probe UHV-STM (*2*), a very stable LT-UHV-STM (*3*), a preparation chamber (*4*), and the UHV transfer-printer chamber (*5*)

surface deteriorates within minutes in ambient conditions. Therefore, an in situ solution was required to keep an atomically clean environment, and the transfer-printer was to be integrated as part of the UHV multi-probes system. As a consequence, the growth of the Au nano-islands on the MoS_2 stamps must also be performed in UHV using different evaporator and heater settings compared to the growth under clean room conditions.

Our UHV transfer-printer is developed around a single Attocube high-resolution piezo-positioner (ANPZ101 with a 5 mm range) [5] as the main mechanical element as shown schematically in Fig. 2 below. The Attocube piezo-stack is translated by a

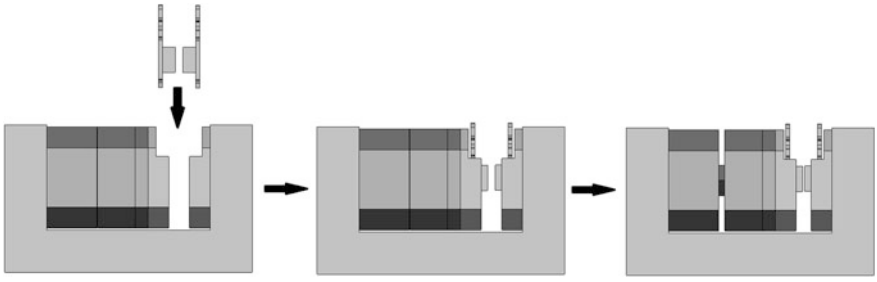

Fig. 2 Concept of the transfer-printing technique using a single Attocube piezo-positioner to receive the sample (*left*), bring the stamp, and the receiving sample into contact (*right to left*). The rest of the components are made in UHV-compatible materials, mainly stainless steel 316LN

stick-slip motion with a maximum force of 5 N. This limits the pressure during the transfer-printing process and ensures minimal damage to the sample where the Au metallic nano-islands are going to be soft transfer-printed.

The printer presented in Fig. 2 above includes a few modified parts as compared to the original one in air, specifically the plate holders. Original plate holders were only equipped with one spring that, if used in the new UHV-compatible printer design, would have induced a tilt of the sample as pressure is applied by the nano-positioner. Therefore, a second set of springs was introduced in order to keep the sample plate in a vertical position while offering some leeway in the horizontal placement as shown in Fig. 3. This is an important change for a transfer-printing

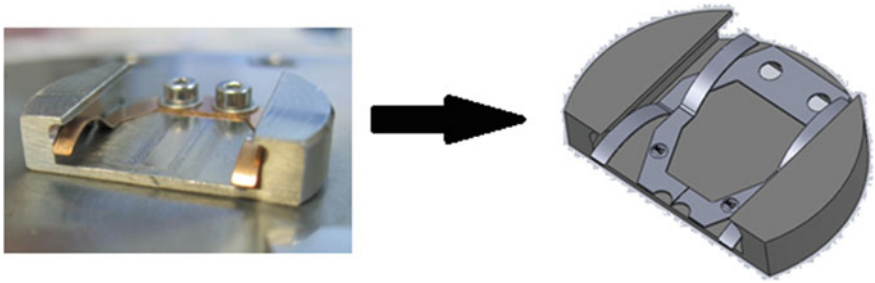

Fig. 3 *Left* Original plate holder with only one set of springs. *Right* Schematic of the modified plate holder with a second set of springs spot welded to the holder in order to provide better stability to the sample holder during printing. The whole setup shown in Figs. 2 and 3 can then mounted on a 6″CF flange with the required UHV-compatible electrical feed through to control the Attocube setup as shown in Fig. 4

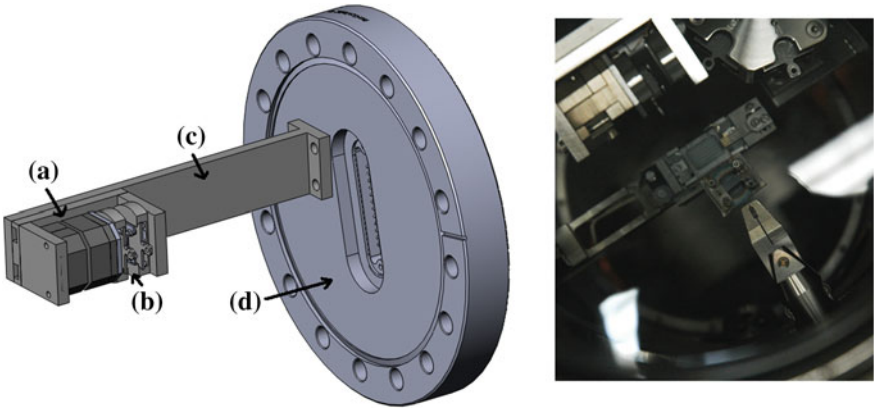

Fig. 4 *Left* Schematic of the transfer-printer setup with its Attocube system (*a*), the sample plates inserted (*b*), the main holder (*c*) and the 6″ CF flange with an electrical feed through (*d*). *Right* Photograph of the live system in the printer chamber with the manipulator used to load the samples on the transfer-printer

process since the springs can compensate for a slight tilt of the sample and ensure a precise parallel alignment of the substrates when pressure is applied. Furthermore, the specific design of the Omicron UHV sample holder restricts from using a plane Omicron sample plate. Therefore, dedicated sample plates were designed with an elevation to mount the substrate (as presented on the Fig. 2 cross section).

3 Transfer-Printing in UHV

3.1 MoS_2 Pillar Fabrication

The MoS_2 wafers were fabricated from large-size bulk molybdenite material mined in Australia. Freshly cleaved MoS_2 surfaces with a maximal number of large terraces were prepared prior to the patterning process by a combination of photolithography and reactive ion etching (RIE) in a standard clean room environment. A 2-µm-thick AZ-7220 photoresist film was spin coated onto the MoS_2 wafer. Arrays of squares of 30-µm base were patterned over the entire wafer surface using ultraviolet photolithography. The patterned photoresist was used as a mask to etch pillars into MoS_2 by RIE in SF_6 at 100 W for 6 min. The height of the pillar was adjusted by controlling the RIE etching time. Then, the samples were immersed in acetone to remove the photoresist, leaving very flat squared MoS_2 pillars on the surface. A dip in piranha solution (3:1 H2SO4:H2O2) for 10 min removed any organic residue before loading the samples either in the gold thermal evaporator for ex situ growth or in the UHV multi-probe system for in situ growth of the Au nano-islands. In both cases, the MoS_2 wafer stamp needs to be pumped at least during 48 h in for the MoS_2 surface to be clean enough for a UHV environment and to preserve the quality of the Si(100) 2 × 1 H surface which will be printed on.

The sample holder for the patterned MoS_2 is a modified Omicron sample plate with a ∼3-mm-high cube with mechanical grips on the side to allow room for the transfer-printing to be done. The recipient is a silicon piece that was flashed and passivated with hydrogen, and it is held on a sample holder allowing direct heating of the sample. This holder has screws protruding on each side of the sample, and this limits the size of the patterned MoS_2 in one direction. The lamellar structure of the MoS_2 stamp renders the contact very soft due to the bulk lamellar structure absorbing large amounts of contact pressure.

3.2 Characterization of the Transfer-Printed Samples

To “ink” the MoS_2 stamp that is to grow Au nano-islands on the surface of each MoS2 pillar, the patterned MoS_2 sample is inserted into the printer chamber of the Fig. 1 UHV machine and heated at 400 C in a base pressure of 10^{-9} mBar. Then, a

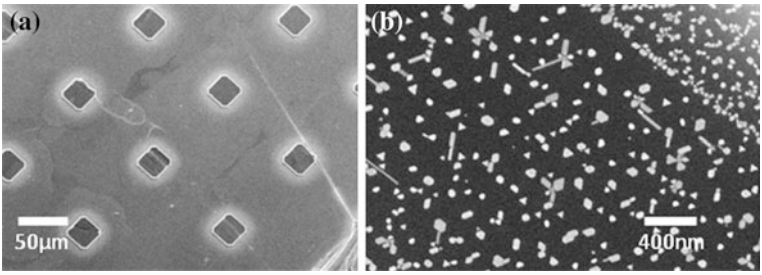

Fig. 5 **a** SEM images of the patterned MoS_2 sample with in situ deposition of 1 nm of gold by thermal evaporation. **b** High-magnification SEM image showing the presence of well-defined gold islands. Images were taken at 15 kV and 400 pA probe current with 13.4 mm working distance. Images obtained in situ in Fig. 1 UHV-SEM available in the interconnection machine

layer of 1 nm of gold in thickness (measured on a quartz crystal monitor) is evaporated from a thermal evaporator. As presented in Fig. 5 and in this environment, Au nano-islands can still be formed but with a lesser yield of triangular islands formation than when this evaporation is done ex situ [4]. On a side note, e-beam evaporation in UHV had also been tried. But for unknown reasons, it resulted in much less Au crystalline nano-island formation on the surface than a standard thermal process. One interpretation is that depending on the e-beam dose, the MoS_2 surface of the pillars is damaged by the e-beam exposure leading to a more difficult Au atom diffusion on the MoS_2 surface.

In parallel, the Si(100) sample was flashed numerous times up to a temperature of 1200 °C in the preparation chamber of the Fig. 1 machine to achieve an atomically flat surface. This was followed by hydrogen passivation using a hydrogen cracker [6]. The two samples are then brought in the UHV printer chamber always maintained in an UHV environment during the complete transfer and are ready for the printing process.

The MoS_2 sample is approached in close proximity to the Si(100)H surface using the Attocube positioner. The stick-slip motion is achieved using a voltage of 30 V with a repetition rate of 200 Hz. The samples are deemed in contact when an audible change in frequency is heard and the motion is stopped. The piezo is then fully extended by ramping up the DC voltage up to 60 V to ensure a full contact. The system is kept with these parameters for 5 min. The voltage is then decreased to 0 V, retracting the MoS_2 sample from the hydrogen passivated silicon surface. Backward coarse motion retracts the Attocube fully to its standby position, allowing the retrieval of the Si(100)H sample and its UHV transfer to the SEM in the multi-probe chamber of the Fig. 1 machine to confirm the success of the transfer-printing.

To be able to identify small portions of printed area with ease, SEM is a strict requirement. Due to the natural roughness of the MoS_2 and the less than ideal alignment of the samples, the transfer mostly occurs at specific spots, generally near the edge of the MoS_2 sample which often has a raised profile due to the cutting of

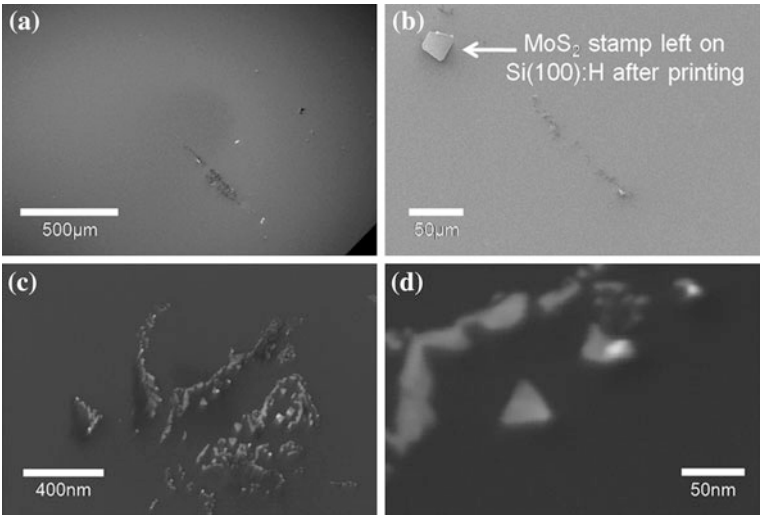

Fig. 6 SEM images of the hydrogen passivated silicon sample after the printing process. **a** A low magnification SEM image shows impacts on the substrate, where most likely transfer of the nano-islands happened. **b** Further magnification shows that part of a pillar has also been transferred. **c** After further search, transferred islands can be found, with further magnification in panel d. Images were taken at 10 kV and 400 pA probe current with 14.8 mm working distance

the sample. Nonetheless, printing is effective for most samples, and area with triangular Au nano-islands can be found as presented in Fig. 6. The printing process is causing damage to the MoS_2 stamp (some pillars are even transferred entirely as shown in Fig. 6b), and they generally last for only one printing operation.

Using the high-resolution probe of the UHV-STMs of the Fig. 1 multi-probe STM head, the transferred Au nano-island can be further imaged. The comparison between such an STM image and the exact same Au nano-island UHV-SEM image is presented in Fig. 7. It is very important here to notice the unique feature of the Fig. 1 complete UHV machine to be able at the same time to deliver an UHV-SEM image with a precision of about 4 nm, to precisely locate the surface area SEM imaged and to position the STM tip apex of the high-resolution probe exactly on this area. Using the STM tip, attempts were also made to manipulate a single Au nano-islands on the Si(100)H surface following the procedure introduced by Yang et al. [7]. This was not successful so far, and work is in progress to fine-tune the parameters to achieve manipulation on the Si(100)H surface as compared to the original MoS_2 surface. Electronic dI/dV STM spectroscopy measurements on and away from a single Au nano-island have also been carried out and show different behaviors: A full characterization is underway, and the results will be reported elsewhere.

Note that in Fig. 7, atomic resolution was not achieved on the Si(100)H surface after and even before the transfer-printing step. The sample has to be transferred to the low-temperature STM attached to the multi-probe chamber to characterize the

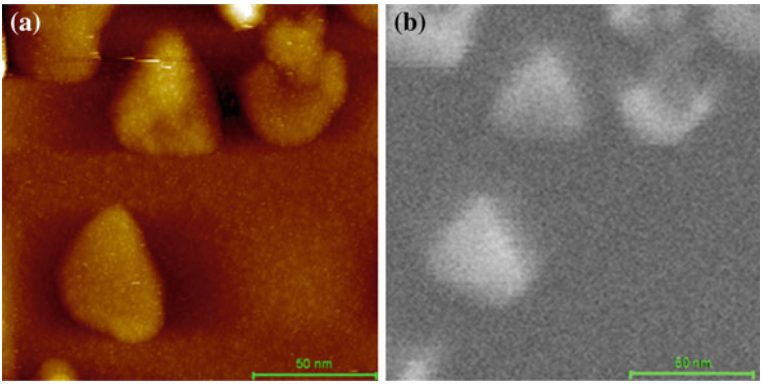

Fig. 7 **a** UHV-STM image and **b** UHV-SEM image of the same area showing the exact correspondence between the two images

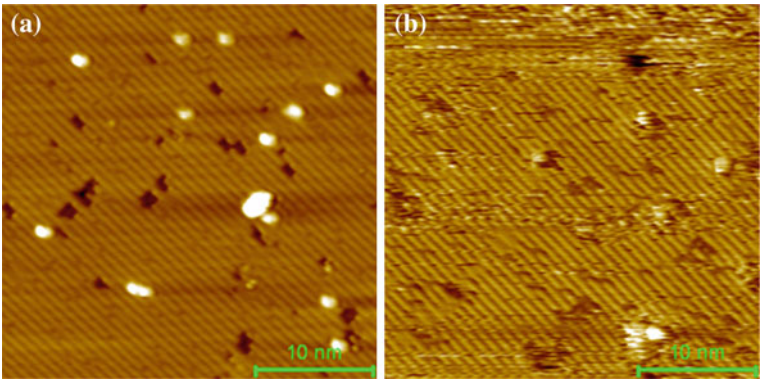

Fig. 8 STM image of Si(100):H **a** before and **b** after printing of Au nano-islands from the MoS_2 stamps. The images were obtained by scanning at a bias voltage of −2.5 V and a tunneling current of 20 pA on the LT-STM of the multi-probe system

surface with an atomic resolution. However, when the sample is transferred to the single-probe STM, it becomes very hard to find the printed area due the absence of an SEM. Nevertheless, one attempt was successful, and one could see that the area surrounding the islands is damaged by friction between the 2 surfaces during the printing process. Once the STM tip is moved further away from the area of mechanical contact, silicon reconstruction is recovered as shown in Fig. 8, indicating the destructive impact of the printing process is much localized.

4 Conclusion

As the need arises to get single nano-crystals on a surface onto which these nano-crystals cannot be grown naturally, or deposited conveniently without compromising the cleanliness and atomic ordering of the surface, we provide here an amenable solution in UHV. A nano-positioner based on stick-slip motion can bring together a stamp, here a MoS_2 sample with single-crystal Au nano-islands formed upon Au deposition, and a receiving surface, for instance an atomically clean hydrogen passivated silicon surface, together with a force of 5 N to transfer, or print, some of the nano-crystals onto the silicon surface while preserving the atomic cleanliness, at least away from the deposited crystals. These first steps have been demonstrated successfully, but improvements are needed which would ensure a facile motion of the nano-crystals on the recipient surface. As it stands, the transfer process is rather harsh and refining the landing of the stamp on the recipient could be favorable. The advantages of this process are numerous as it would allow studying the interaction of materials or elements, like polymer ribbons, at the atomic scale which would not be possible using normal deposition techniques.

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Site-Selective Self-Assembly of Nano-Objects on a Planar Substrate Based on Surface Chemical Functionalization

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Abstract Surface chemical functionalization is a powerful tool to bridge the gap between top-down and bottom-up nanofabrication methods. By tuning their surface chemistry, we can enable whole sets of different nano-objects to be selectively deposited onto well-defined submicronic anchoring sites on macroscopic substrates. This potentially enables the development of unprecedented systems in different fields such as electronics, photonics or biosensors.

1 Introduction

Information processing technology relies nowadays on manufacturing of micro-nanosystems (e.g. electronic [1, 2] or photonic components [3]) using top-down fabrication. Besides, fabrication of new elementary objects based on bottom-up chemical synthesis can lead to molecules or nano-objects with exotic properties, such as molecular switches [4, 5], biomolecular origami [3], multifunctional

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DOI 10.1007/978-3-319-21194-7_7

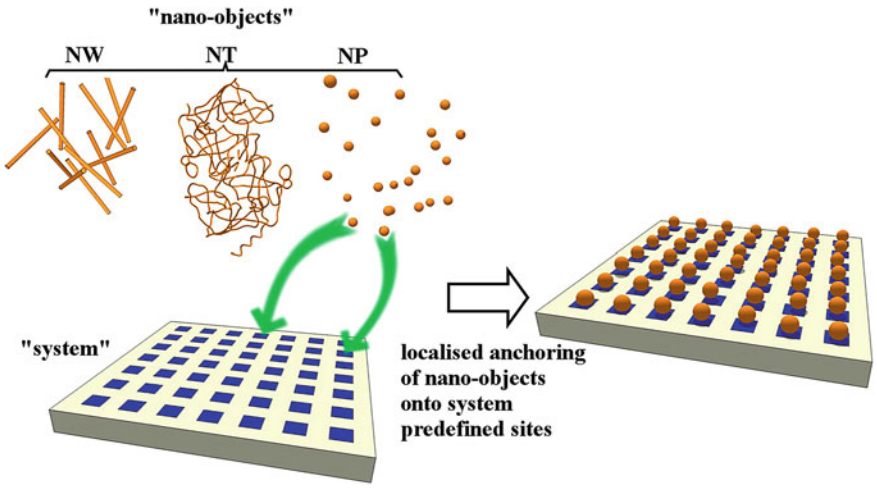

Fig. 1 Fabrication of devices by combining the synthesis of a set of nano-objects (e.g. nanoparticles NP [12], nanotubes NT [13] or nanowires NW [14]) and a system (e.g. photonic or electronic component, aimed at processing information or detecting events, such as a sensor) with specific sites on which nano-objects should be anchored. The collective anchoring of nano-objects onto the adequate sites of the system may provide an approach for designing new devices with exotic properties, uneasy to fabricate with classical top-down processes

particles [6–8], nanocrystals or nanowires. Associating such different fundamental entities (e.g. single molecules, nanocrystals or nanowires) for the implementation of hybrid devices is envisioned to yield functionalities exceeding those of the individual subunits in different fields such as electronics [9, 10] or nanophotonics [11]. Creating new heterogeneous components can be explored by associating presynthesized sets of nano-objects onto a system previously created using a top-down approach (see Fig. 1). Combining top-down and bottom-up approaches, complementary strategies may indeed yield devices with new functionalities. However, correctly addressing batches of nano-objects onto predefined sites of an electronic or a photonic system involves many challenges: addressing efficiency, compatibility of each fabrication step with the global process, packaging and storage constraints. We present herein some possibilities and limitations of collective addressing of an ensemble of nano-objects onto a system, based on surface interactions.

To ensure the chemical anchoring of each nano-object onto the planar substrate, the chemical groups at the surface of the nano-object should "match" the chemical groups at the surface of the substrate. This can be achieved either by using the intrinsic surface moieties of the different materials or by modifying it in a process called *surface functionalization* (see Fig. 2).

In this chapter, we will review different methods for binding an ensemble of nano-objects onto a planar surface by surface functionalization based on

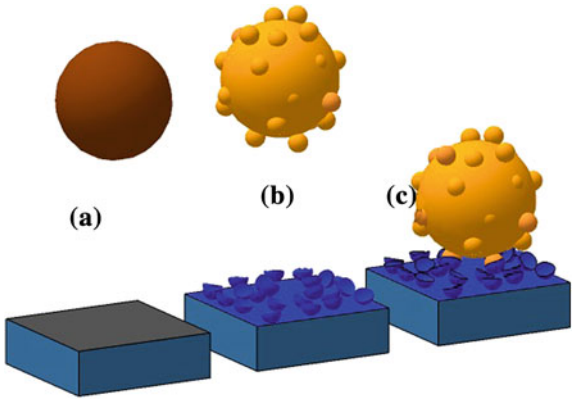

Fig. 2 Surface functionalization to bind a nano-object onto a surface. The bare substrate and nanoparticle (**a**) are modified with complementary chemical moieties (**b**) that allow the binding of the nanoparticle on the substrate (**c**)

electrostatic forces, covalent binding and/or biomolecular affinity. Assembly by an applied external field (e.g. optical trapping or dielectrophoresis) is thus excluded from this review, although such techniques can be used in combination with surface functionalization [15]. Furthermore, we will also investigate different approaches for the chemical patterning of the substrate. Chemical patterning can be used to define specific micro- and nanometric sites for anchoring the nano-objects, as opposed to their self-assembly on a homogeneous surface (e.g. colloidal crystals or opals) which falls out of the scope of this chapter.

2 Nanoparticle Binding

As seen in Fig. 2, intermolecular forces can be used to bind a nanoparticle[1] onto a planar substrate by "matching" the surface chemistry of both. Different interactions can take place between the two surfaces. We will focus on three different interactions that can be tuned by an appropriate surface chemistry as well as the nature of the medium (solvent) in which the interaction occurs. First, we will investigate the use of electrostatic binding, then covalent binding (chemical bond between the particle and the substrate) and finally biomolecular affinity.

[1]Unless otherwise specified, the term "nanoparticle" will be used in the present text as a generic term for various types of nano-objects such as spheres, rods, wires or tubes of different materials.

2.1 Electrostatic Interaction

Surfaces, as well as molecular species in an aqueous or organic solution, may be electrically charged by different phenomena [16]. In aqueous solution, surface electric charge of materials depends on the nature of the surface chemical moieties and on the ionic species in the liquid phase; among these ions, hydronium H_3O^+ and hydroxide HO^- determine the pH of the solution and the acid/base state of the surface. Other ions determine the solution's ionic strength and electric screening phenomena at the solid/liquid interface. This screening effect is related to the so-called Debye length. The pH at which the net surface charge turns from positive to negative is called in the present text "point of zero charge" (PZC). The reader is invited to read the following references for deeper understanding of the phenomena involved with this concept [17, 18].

Two methods can be used in order to bind particles onto a substrate through electrostatic interactions: (i) using the intrinsic surface chemical moieties of the substrate and/or the particle; (ii) modifying the surface chemical moieties of the substrate and/or particle via surface functionalization. The first solution is obviously simpler as long as the involved materials provide the adequate chemical moieties. The second approach is more versatile as it enables to graft virtually any surface chemical moiety on a large diversity of materials. However, functionalization implies additional steps and has to be compatible with the constraints of the materials and finalized systems (e.g. relative robustness of the transducer in the design of a biosensor). We give below examples of both strategies.

2.1.1 Using Intrinsic Material Properties

In some cases, the surface charge of the substrate and the particle's materials in a given medium may be directly used to perform the appropriate electrostatic binding between the two.

Figure 3 shows silicon nanowires immobilized onto SiO_2 substrate with Si_3N_4 sites. Sketch (a) summarizes the structured substrate's organization. Si NWs were

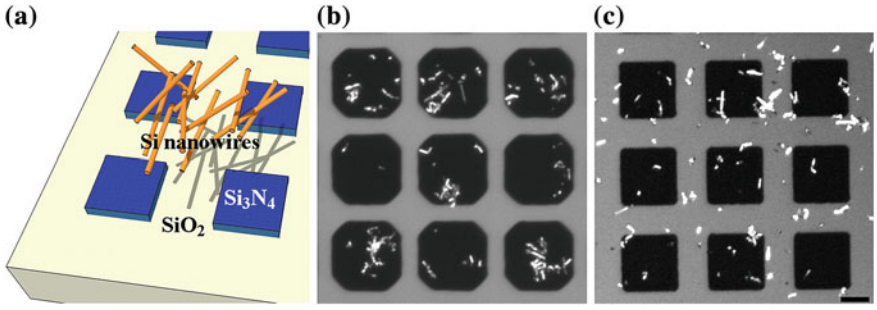

Fig. 3 Selective coating of Si nanowires onto SiO_2/Si_3N_4 substrate. Scale bar = 10 μm

spread onto a substrate in aqueous solution with a controlled pH. NW solutions were washed with an aqueous solution of same composition (salts, pH), while carefully avoiding any drying of the liquid on the substrate as long as wires were present in the liquid phase. Capillarity was thus unable to be the main force driving interactions between nanowires and the substrate. Pictures (b) and (c) are optical microscope images of nanowires immobilized onto substrates after washing and drying. Substrate (b) was obtained with a pH between the points of zero charge of SiO_2 and Si_3N_4. The two materials exhibit, respectively, negative and positive surface charge, causing Si nanowires (due to their thin native SiO_2 layer) to interact more robustly with Si_3N_4. Sample (c) was obtained with a different pH. In this case, nanowires interact in similar ways with SiO_2 and Si_3N_4 so that no selective anchoring takes place. Si nanowires were provided by Laboratoire des Technologies de la Microélectronique. [14, 19]

2.1.2 Using Surface Functionalization

Surface functionalization can tune electrostatic forces between a nanoparticle and a substrate by controlling their charge in a given environment.

Two of the most commonly used terminal groups for electrostatic binding are carboxylic acids and amine groups. In their neutral form, their formulas are, respectively, –COOH and $–NH_2$. However, the pKa of $CH_3–COOH/CH_3–COO^-$ is around 4.7, while the pKa of $CH_3 - NH_3^+/CH_3 - NH_2$ is around 9.9, so that for a given range of pH (ca. 4.7–9.9), carboxylic acids will be mainly deprotonated to COO^- and amines mainly protonated to NH_3^+. This results in an attractive electrostatic interaction between the two chemical groups.

Gold nanoparticles are commonly capped with citrate moieties bearing a negative charge in most conditions, coming from carboxylate end groups. This is used primarily as a way to stabilize the colloids, avoiding the particles' aggregation. Nonetheless, the negative charge of the citrate can be used to attach the particle to a positively charged substrate. This methodology has been used to bind gold nanoparticles to amino-functionalized surfaces of different materials such as gold [20], silicon or silica [21, 22] and ITO [23]. Gold nanoparticles have also been electrostatically bound to a silica substrate whose surface charge was tuned by an ion beam [24]. Gold is not the only material conventionally functionalized with carboxylic acids. Polymer and silica beads can also easily present carboxylates COO^- used to bind the nanoparticles to amino-functionalized regions of a substrate [25].

Conversely, it is also possible to bind amino-functionalized nano-objects onto naturally negatively charged surfaces. This has been reported with silicon nanowires functionalized with APTES[2] bound onto negatively charged bare gold or silica [26]. In this case, it was also possible to repel the nanowires from the

[2]Aminopropyltriethoxysilane.

substrate by functionalizing the latter with methyl-terminated (neutral charge) molecules (OTS[3] on silica or ODT[4] on gold).

A similar use of self-assembled monolayers was made by Arpin et al. [27]. In this case, micelles containing a positively charged surface of PVP[5] are assembled via capillary forces into submicronic holes on a silica substrate. However, capillary forces alone do not ensure site-selective deposition, as non-specific adsorption of the micelles on the surface between the holes remains important. To solve this, an amino-terminated self-assembled monolayer (SAM) is deposited in the space between the holes to repel the micelles by electrostatic interaction.

Eventually, oligonucleotides can also be used as negative charge-bearing molecules for electrostatic binding. Though the use of oligonucleotides usually implies a biological recognition (DNA/DNA hybridization, see Sect. 2.3), the intrinsic negative charge of a DNA strand at the surface of a nanoparticle can be used to bind that nanoparticle onto a positively charged substrate. This was used by Zheng et al. [28] as a first step in a complex nanoparticle array "printing" set-up combining electrostatic interactions and biological recognition. In that paper, gold nanoparticles bearing negatively charged DNA strands at the surface were first self-assembled from an aqueous solution onto positively charged amino-functionalized silica. In a second step, a planar substrate functionalized with the complementary DNA strand was brought in contact with the electrostatically bound nanoparticles to detach them from the silica surface and attach them to the second substrate by DNA/DNA hybridization (see Sect. 2.3).

We have seen how electrostatic binding can be applied to the anchoring of nano-objects on a substrate. Positive surface charges are often obtained by amino-functionalization [20–23, 26–28], whereas negative charges can be either found "naturally" on the surface (silica, gold at pH = 7 [26]) or further enhanced with carboxylic acids [20–23] or oligonucleotides [28] among other molecules. Furthermore, functionalization can play not only an active role in substrate–particle binding but also a repellent role, to avoid non-specific adsorption [26, 27].

2.2 *Covalent Binding*

Electrostatic interactions (see Sect. 2.1) are easy to implement and adjust by modifying the pH of the colloidal dispersion. However, these interactions are weak, meaning that the particles attached to the substrate in this fashion can be easily removed and may not withstand necessary washing steps, sonication or other processes that may be needed. Thus, covalent binding may be preferred for robust attachment of nanoparticles onto the substrate.

[3]Octadecyltrichlorosilane.

[4]Octadecanethiol.

[5]Polyvinyl pyridine.

We have already mentioned the use of COOH–NH_2 (or $COO^- - NH_3^+$) pair for electrostatic binding. However, based on this pair, it is also possible to create an amide bond (O=C–NH) for covalent coupling. This requires the "activation" of carboxylic acids with a carbodiimide and/or succinimide [29].

Covalent coupling via amide bond has been reported for the immobilization of nanoparticles on precise locations of a solid substrate [30–32]. In this case, it might be the substrate that is functionalized with carboxylic acids and the particle is amino-functionalized [30, 31] or the opposite [32].

In the case of gold and, to a lesser extent, other metallic surfaces, functionalization is usually carried by thiols (mercaptans), that is organic molecules with a sulfhydryl headgroup. A molecule with thiol terminal groups at each end of the spacer chain (dithiol[6]) can be used to bind gold nanoparticles on gold [20, 33, 34]. This has proven to be efficient in the building of single-electron transistor with a gold nanoparticle (coulomb island) self-assembling through decanedithiol between two gold electrodes [34]. Other results report the binding of different magnetic particles (Co, Ni, Fe) onto gold through dithiols and catechols [35].

Other functionalizations are reported to bind different kinds of nanoparticles onto different substrates. For instance, Yildirim et al. [36] selectively attached FePt nanoparticles stabilized with oleic acid or oleyl amine through ligand exchange onto ABP[7]-functionalized alumina.

Covalent binding requires the use of material-specific headgroups and may need additional steps compared to electrostatic binding (e.g. activation of COOH groups). However, covalent binding results in a stronger, hence more robust anchoring than electrostatic binding.

2.3 *Biomolecular Recognition*

Biomolecules can be very useful for anchoring nanoparticles on a substrate. Indeed, biological systems such as DNA/DNA, antigen/antibody or biotin/avidin are known to be highly specific.

Oligonucleotides (DNA, PNA, RNA) can be used to immobilize particles on a substrate, via hybridization. This method has been successfully employed to bind gold nanoparticles to gold regions of a substrate [28, 37, 38] but also magnetic particles onto patterned silica [39]. In the case of Lalander et al. [37] and Zheng et al. [28], the immobilization was carried through a third oligonucleotide binding simultaneously the DNA strands on both: the substrate and the nanoparticle. In the case of Anstaett et al. [38], in addition to the PNA/PNA interaction, the rest of the

[6]Dithiol is used in this case for a molecule having a thiol group at each extremity of an alkyl chain, whereas it can also be used in the literature for a molecule having two thiol groups at one end of the alkyl chain.

[7]aminobutylphosphonic acid.

substrate was passivated with a PEG–silane to further diminish non-specific adsorption.

Other than oligonucleotide hybridization, biotin/avidin interaction has also been used for the selective binding of nanoparticles onto patterned substrates [39, 40].

Biochemical binding can be specially useful in an application that requires a reversible anchoring of the nano-objects. Indeed, biological interactions are often temperature- or pH-dependant. DNA/DNA hybridization, for instance, can be reverted by heating over a "melting temperature" that can be computed for a given strand. However, surface functionalization with biomolecules usually involves a prior chemical functionalization of the surface, unless using previously modified biomolecules, such as thiolated DNA for gold functionalization [37].

2.4 Nanoparticle Binding Strategies: Summary and Comparison

We have reviewed so far three different kinds of interactions reported in the literature to bind nano-objects onto a substrate: electrostatic binding, covalent binding and biochemical binding. Though the three methods are indeed used to bind different nano-objects onto a variety of substrates, they do not have the same advantages and drawbacks. From a user point of view, it might be interesting to compare these methods regarding the *strength and robustness* of the bond between the substrate and the particle, the *specificity* of this bond and general *simplicity* or ease of use of the method (see Table 1).

Strength and robustness: Different applications may require the nano-objects to be more or less strongly bound onto the substrate. Indeed, after immobilization of the particle, the sample may undergo different washing steps including sonication and be exposed to different media (aqueous solvent, organic solvent, air, vacuum, etc.). It is then important to know the strength of the bond between the particle and the substrate. Generally speaking, covalent bonds are stronger than electrostatic bonds. Au–S bond, for instance, has a free energy around −50 kcal/mol [41], whereas electrostatic bonds are typically around 1–10 kcal/mol. Furthermore, electrostatic (ionic) bonds are highly dependant on the pH and ionic strength of the solution. Similarly, biochemical interactions such as DNA/DNA hybridization or biotin/streptavidin linkage are mainly based on weak interactions, such as hydrogen

Table 1 Indicative summary of different binding strategies with main advantages and drawbacks

	Electrostatic	Covalent	Biological
Robustness	Low	High	Medium
Specificity	Low	Medium	High
Simplicity	High	Medium	Low

More details and precise examples about bonds' free energies or conditions for implementing different methods can be found in the text

bonding. Hydrogen bonds are typically also in the 1–10 kcal/mol free energy range. However, the number of bonds also needs to be taken into account. Some studies [42, 43] suggest that polythiols can anchor onto gold in a more robust way than monothiols. Conversely, in DNA/DNA hybridization, two or three hydrogen bonds are created between each pair of complementary bases leading to a high number of hydrogen bonds between oligomers; furthermore, stability of DNA duplexes is also ensured by pi stacking between adjacent nitrogenous bases. Indicative free energy for oligonucleotide duplexes is between −10 and −20 kcal/mol [44], while streptavidin–biotin complex exhibit a free energy of around −18 kcal/mol [45]. Nonetheless, as mentioned before, nucleic acid dehybridization and protein denaturation can easily occur when heating or changing ionic composition of the medium, so that binding based on biomolecular affinity (or ionic bonds) may be less robust than covalent coupling.

Specificity: In the case where different nano-objects and/or different substrates are used, surface functionalization may be required to be as specific as possible so that only the "right nanoparticle" is immobilized onto the "right substrate". For this purpose, biological systems often have great specificity because they are based on a variety of complementary interactions combining hydrogen bonds, hydrophobic interactions and geometrical "matching" among others. Thus, a given DNA strand or an antibody will be highly specific of the complementary DNA strand or the antigen. Covalent binding can be quite specific in some cases too, as some chemical groups will specifically bind some materials (e.g. thiols on metals or silanols on oxides). However, a thiol headgroup may well bind different metals without discrimination. Similarly, an activated NHS ester will bind an amine group but will not discriminate between two different amino-functionalized particles. Eventually, electrostatic bonding may be considered the least specific method, as any electric charge will attract an opposite charge.

Simplicity: Though it is difficult to give an estimate of the needed time and number of steps for each method, we can say in general terms that electrostatic binding is easier to implement than covalent binding, itself being generally easier to do than binding through biological interaction. Indeed, electrostatic binding may not require grafting additional molecules (SAM) on the surfaces [24]. If a SAM is used, it is usually formed in one single step and only the pH (and depending on the case also the ionic strength) of the medium in which the interaction occurs has to be controlled. Covalent binding may require additional steps, such as activation of carboxylic acids when the COOH–NH2 couple is used. This activation and the ensuing covalent coupling may require more specific conditions regarding the medium [29] making it less straightforward than electrostatic binding. Eventually, binding based on biological interactions is usually more complex to implement. First, it usually requires more functionalization steps, as the biomolecules are rarely directly attached on the surfaces, so that a prior chemical functionalization is needed. Second, biological interactions often require a very controlled environment regarding pH and salinity (buffer) as well as temperature.

3 Chemical Patterning

We have seen in the previous section that nano-objects can be attached onto a planar substrate through different forces. These forces, based on electrostatics, chemical covalent binding or biochemical recognition, can be tuned by modifying the surface moieties of the nano-objects as well as the substrate's (surface functionalization). Among different functionalization methods, it is common to graft molecules on the surface (rather than working directly on the chemical moieties intrinsically present, which remains an option nonetheless [24]). These molecules may have different degrees of ordering and close-packing, ideally forming self-assembled monolayers (SAMs). It should be noted, however, that this "ideal" case of well-ordered close-packed reactive groups may not always be the most effective case in order to bind molecules or particles from the solution [46–48]. SAMs can be built on a wide range of materials in mild conditions (room temperature, atmospheric pressure, from aqueous solution, organic solvent or gas phase). A SAM is typically made of molecules presenting an alkyl or alkyl polyethylene glycol spacer between two terminal groups: one being specific of the substrate's material and the other having a specific function, in this case, to bind a nano-object. Furthermore, as noted in the introduction of this chapter, many applications require a *site-selective* deposition of the nano-objects onto the substrate rather than a homogeneous deposition on the whole surface. This means that, for a given surface chemistry of the nano-object, the planar substrate has to be chemically patterned, in order to have binding sites with "complementary" chemical groups ("stable interaction") surrounded by a repelling surface of "non-complementary" chemical groups ("unstable interaction") (see Fig. 4).

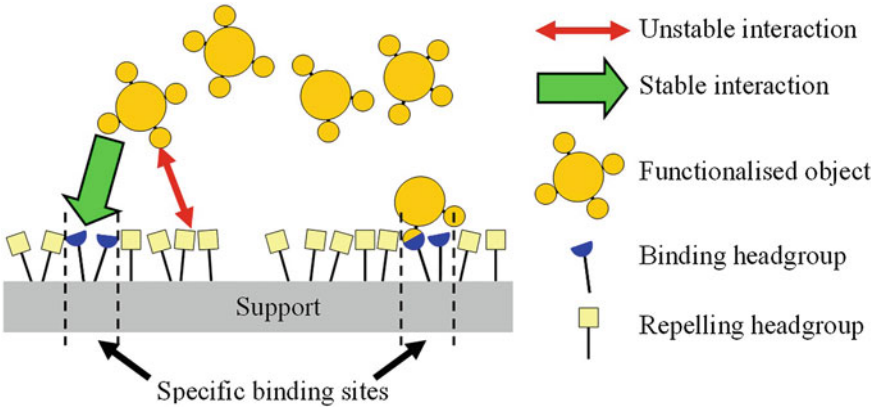

Fig. 4 Site-selective deposition of nanoparticles on a chemically patterned substrate

There are several ways to chemically pattern a solid substrate:

1. A SAM can be printed onto given regions of the substrate with a topographically patterned stamp (microcontact printing) [20, 30, 32, 33, 35, 36]. Alternatively, it is possible to use a flat stamp on a topographically patterned substrate [27]. The remaining regions of the substrate can be later functionalized with a second SAM (back-filling).
2. Patterns created by lithography on a polymeric layer (photo- or e-beam resist) can create openings for a SAM to form only at given regions, as in a standard deposition/lift-off process (where the "deposited material" would be the SAM) [22, 25, 49]. After dissolution of the resist, the rest of the surface can be backfilled with a second SAM.
3. A homogeneous surface (bare substrate or homogeneous SAM) can be modified at specific regions either by altering the chemical groups with an electron or ion beam (direct writing) [24] or by means of photolithography [50]. Furthermore, a SAM can be deposited via an AFM tip (dip-pen nanolithography) only at precise locations of a bare substrate [30].
4. A substrate previously patterned with different materials (e.g. gold nanostructures on a silica surface) can be selectively functionalized with molecules that self-assemble onto one or the other material [34]. Alternatively, the intrinsic chemical variation given by the different materials can be used without further functionalization.

3.1 Microcontact Printing

Microcontact printing (μCP) was first developed by Kumar and Whitesides in 1993 [51]. It consists in "printing" a SAM onto given regions of the substrate with a topographically patterned stamp. This stamp, usually made of PDMS, is first brought in contact with the solution containing the molecules of interest (ink) and then applied onto the substrate to transfer the above-mentioned molecules that form a SAM only at the regions defined by the topography of the stamp [20, 30, 32, 33, 35, 36], as presented in Fig. 5.

This procedure has been used for the purpose of defining precise binding sites for nano-objects on different materials: alumina [36], gold [20, 30, 35] and silica [27, 32], among others. Typical sizes and periodicity of the features for this application range from hundreds of microns [35] to a few microns [30] though a submicrometer feature size has already been reached [53].

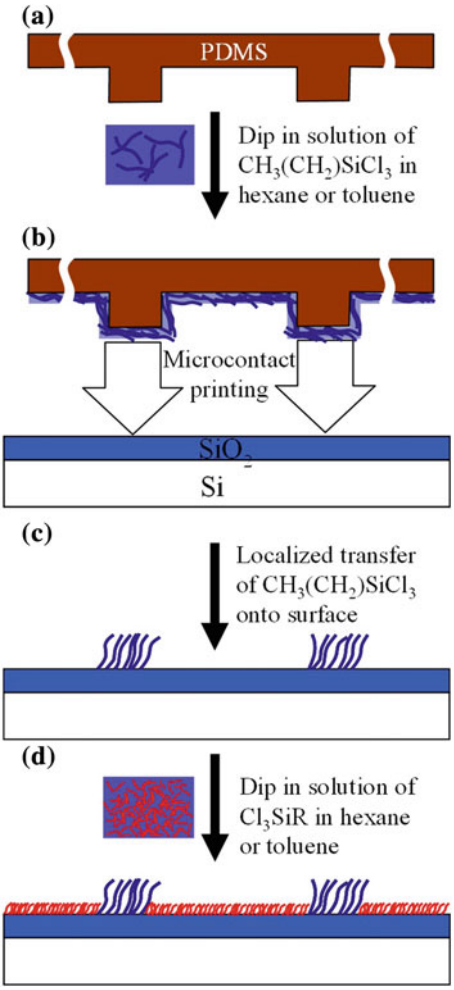

Fig. 5 Microcontact printing of a SAM, followed by backfilling with a second SAM. Adapted from [52]

3.2 Masked Functionalization: "SAM Lift-off"

An option for site-selective surface functionalization is to mask the substrate with a resist that will be patterned by lithography (UV, e-beam or nanoimprint, for instance). Then, a SAM can be formed on the openings of the resist only, with molecules possibly adsorbed on top of the resist elsewhere. The resist is then dissolved leaving the SAM at the predefined locations as in a standard lift-off procedure [21, 22, 25, 26, 49] (see Fig. 6). As with microcontact printing, the regions on the substrate that were not functionalized on the first step can then be further backfilled with a second SAM.

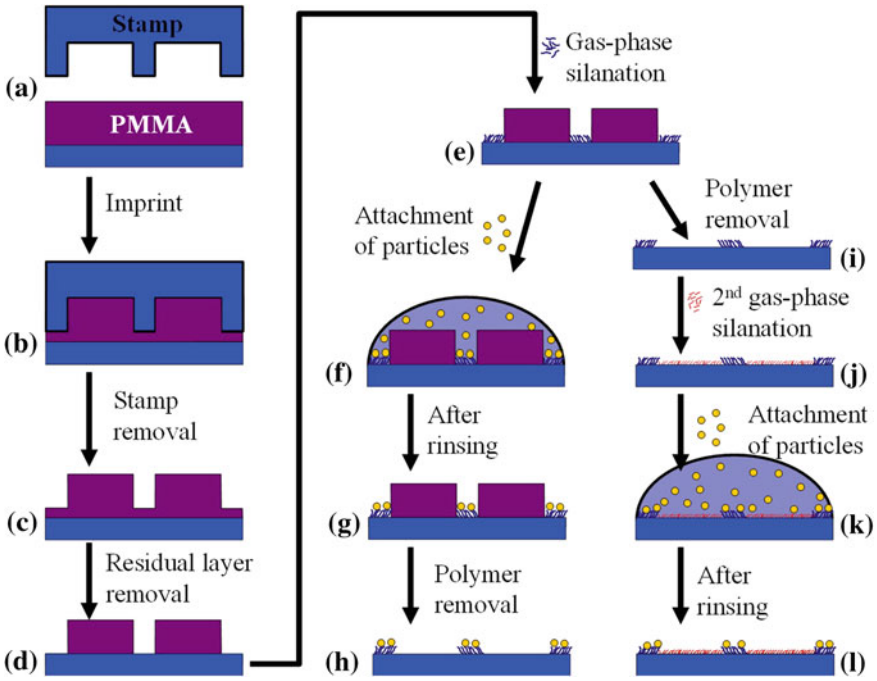

Fig. 6 Controlled SAM formation through the use of a resist mask patterned by (nanoimprint) lithography. Adapted from [25]

Heo et al. [26] used photolithography to pattern gold and silica substrates with methyl-terminated SAMs. In this case, it is interesting to note that the functionalization was done to repel the nano-objects (functionalized silicon nanowires) which were bound on the regions where no SAMs were formed.

In another interesting approach developed by Maury et al. [25], nanoparticles were made to assemble at the functionalized regions *before* dissolution of the resist.

Nanoimprint lithography [22, 25] as well as e-beam lithography [21] of PMMA has also been used to create local SAMs on silica, to bind gold nanoparticles. With this technique, patternings can be created with a feature size that becomes comparable to the dimension of a single nanoparticle [21].

3.3 Local Modifications of a Homogeneous Surface

Another option for the chemical patterning of a homogeneous substrate is to modify certain regions by photolithography (large areas, high throughput but lower resolution) or by a "local probe" (small areas, low throughput but higher resolution). Different approaches exist:

- Modifying native chemical surface groups with an ion or electron beam [24].
- Modifying a homogeneous SAM on the substrate by e-beam [54, 55] or photolithography [50].
- Forming the SAM by deposition of the solution ("ink") only at given regions with an AFM tip (dip-pen lithography) [30].

Kolibal et al. [24] were able to tune the surface charge of a silica surface at specific regions by controlling the fluence of an ion or electron beam so that the irradiated area yielded an opposite charge to the non-irradiated. When immersed in a colloidal solution of gold nanoparticles (20 nm diameter) in HF, they could therefore achieve positive and negative grafting (particles adhering to the irradiated or non-irradiated regions) of the particles. The patterns used in this paper ranged from 3 squares to 100-nm dots.

Barsotti et al. [30] used dip-pen lithography to "write" thin lines (less than 100 nm wide) of mercaptohexadecanoic acid SAMs on gold for the subsequent attachment of functionalized gold nanoparticles.

3.4 Chemical Pattern Based on Different Substrate Materials

Eventually, if the substrate is already patterned with different materials, it is possible to functionalize both materials independently, by choosing molecules with the appropriate terminal groups. For instance, thiols (S-H terminal group) will bind onto gold and other metals, whereas silanes (Si-R terminal group) will bind onto silica or other oxides. Alternatively, it is possible to take advantage of the inherent differences between the materials' surface chemistry to trap nano-objects onto one material without further functionalization. For example, by tuning the pH of the solution, one can control the electrostatic attraction or repulsion on materials with different isoelectric points.

Gold nanostructures on silica [56] is quite common as it may have different applications in optics and electronics. Using surface chemical functionalization of these structures may enable the gold nanostructure to "trap" nanoparticles from solution while avoiding non-specific adsorption on the rest of the surface [28, 31, 37, 38]. Using thiolated DNA and PEG–silanes, Udo Bach and co-workers [37] achieved almost single-particle capture with 40-nm beads and less than 1 % of non-specific adsorption (beads adsorbed on silica surrounding gold nanostructures). Beyond the proof of concept, this methodology has already been used in the fabrication of operational devices such as single-electron transistors [34].

Obviously, the same methodology can be applied to other materials, like amino-functionalized ITO [23].

3.5 Chemical Patterning Strategies: Summary and Comparison

We have presented four different ways to chemically pattern a planar substrate for the site-selective immobilization of nano-objects. These methods can be compared in terms of *throughput* (total patterned area per unit time), *resolution* (minimum available feature size and pitch) and *versatility* (available sizes and shapes) (see Table 2):

Throughput: Microcontact printing probably presents the highest throughput of the above-mentioned techniques as an area of several cm^2 can be functionalized in "one go" (less than an hour). Masked functionalization by photolithography has similar throughput, albeit it requires the coating, exposing and developing of the resist mask prior to the SAM deposition. If the mask is patterned by e-beam lithography, then the throughput is greatly reduced as the writing is sequential and can take several hours for 1 cm^2. Local modifications as dip-pen lithography yield even lower throughput and can hardly be used to modify surfaces bigger than 1 mm^2. Regarding patterning based on different materials, the throughput is mainly based on the technology used for creating the mixed substrate as discussed for masked functionalization.

Resolution: As can be expected, resolution and throughput are connected. The techniques with higher throughput such as microcontact printing or masked functionalization by photolithography can hardly reach submicrometer features, whereas techniques based on e-beam or nanoimprint lithography can reach tens of nanometers. Eventually, modification with a local probe has also been used for features smaller than 100 nm.

Versatility: Microcontact printing and other techniques based on photolithography have relatively low versatility, as the same predefined stamp or mask is used on the whole surface. Masked functionalization based on e-beam lithography and modification by a local probe have higher versatility as different shapes and sizes can be defined on the same sample. If the chemical pattern is based on different materials, then versatility is again defined by the technology used to pattern the substrate with the different materials in the first place.

Table 2 Different methods for chemical patterning of a solid planar substrate with indications about main advantages and drawbacks

	Microcontact printing	Masked functionalization	Local modifications	Different materials
Throughput	High	Depending on resolution	Low	Depending on resolution
Resolution	Low	Depending on throughput	High	Depending on throughput
Versatility	Low	Depending on throughput/resolution	High	Depending on throughput/resolution

More details can be found in the text

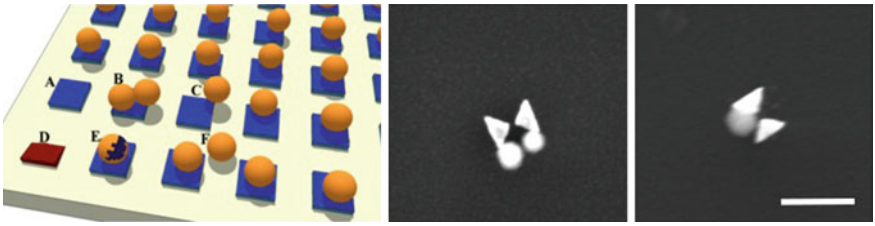

Fig. 7 Fabrication defects associated with anchoring of nanoparticles on structured support. Scale bar for SEM images corresponds to 500 nm

4 Conclusion

Surface functionalization is a very powerful mean to ensure the site-selective immobilization of different nano-objects from a colloidal dispersion onto a planar substrate. This can have many applications in different fields of nanotechnology such as electronics or biosensing devices. Moreover, surface functionalization can bridge the gap between bottom-up built nanoparticles and top-down patterned substrates enabling new methods for nanofabrication.

To achieve low defect systems, one needs to understand deeply the driving forces involve in the positioningof the nanoobjects on the support (see Fig. 7).

The sketch on the left of Fig. 7 provides examples of anchoring defects: (A) empty site, due to inefficient particle transport or ineffective anchoring; (B) multiple anchoring of nanoparticles onto a single site; (C) border effect (e.g. possibly due to capillary forces); (D) and (E) defects of fabrication of support site and particle; and (F) binding of a particle onto a wrong site. The pictures on the right of Fig. 7 provide experimental examples of anchoring: double triangles are gold bow-tie nanoantennas implemented by e-beam lithography onto a silica support [57, 58]. Gold is functionalized with $-NH_2$ functions, while particles bear reactive activated ester functions [59]. Silica support is passivated in order to avoid physisorption of particles. In the tested experimental conditions, particles could be located on the side of bow ties, but not on the top area. These trials illustrate the difficulty to correctly locate nano-objects onto specific sites.

As we have seen throughout this chapter, there are different available strategies to bind a nano-object onto a substrate as well as different strategies to chemically pattern the substrate in order to create specific recognition sites for the nano-objects. We have highlighted the main methods reported in the literature and given their main characteristics, advantages and drawbacks.

Depending on the application, users can choose any of the above-mentioned strategies. As we have shown, different methods may be better suited than others depending on the expected performances: speed, ease of use, resolution, robustness,

etc. Hence, we can expect further implementations on each of the methods presented in this chapter in the following years.

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Silicon Technologies for Nanoscale Device Packaging

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Abstract We present our recent developments on silicon technologies dedicated to the packaging of nano-objects/nano-devices. These technologies aim at both protecting and electrically connecting a nanoscale device positioned on a perfect Si (001)-(2 × 1):H surface smoothed thanks to a 950 °C thermal treatment. The nano-device is connected to nanopads implanted on the silicon surface. Each nanopad is linked to a nanovia which is locally achieved by etching and filling processes operated in a FIB (Focused Ion Beam) equipment. Impacts of the FIB process on via morphology and properties are depicted. Nanopads are fabricated through the local implantation of arsenic, and the effect of the surface smoothing thermal treatment on the dopants diffusion length is estimated by simulation and then experimentally explored. Key process steps such as the etching of a deep cavity and the surface protection with a temporary cap are also described, and a first assembly consisting in a substrate equipped with nanopads and directly bonded with a cap substrate is presented.

1 Introduction

During the last past years, a new research field named "3D integration" has been introduced in microelectronics [1, 2]. This new field aims at increasing the density of functionalities while taking advantage from the interconnection length decrease, leading to both energy consumption and signal delay decreases. The main key process

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that has put forward this technology concerns the "Through Silicon Via (TSV)" development. TSV permits the electrical connection of different components in the third dimension [3, 4]. The devices of the stack are connected together thanks to copper pillars, themselves connected to TSV. Consequently and in order to address higher density of interconnects, this technology now follows a roadmap which consists in increasing the aspect ratio of the TSV. One example for solving this problem is the use of carbon nanotubes (CNT) as TSV [5–10]. They present a higher aspect ratio and a higher conductivity than the copper TSV. This kind of solution is part of a field that could be named "nanomaterials for packaging" which is related to a global "nanopackaging" field [11, 12]. It aims at improving packaging solutions thanks to novel materials as those belonging to the class of nanomaterials. Among them, nanoparticles are also imagined as potential solutions for packaging; the main property that is used in this case is the possibility to achieve an assembly between two parts by a nanoparticle sintering process at a temperature lower than 300 °C. A so-called sintering silver-based Low-Temperature Joining Technology (LTJT) has been developed for die attachment [13–18] or wafer-level bonding [19].

Besides these packaging technologies, a need now appears on the nano-object packaging. One solution, which is today explored in the research laboratories for the fabrication of atomic-scale devices, relies upon the use of the tip of a Scanning Tunneling Microscope (STM) [20]. However, this solution is not suitable for a large production of devices, and technologists are facing a new challenge where the main difficulty is to connect very small objects to electrical connectors, or pads, which means going from the device's scale (atomic or nanometric) to the chip's scale (micrometric). In particular, the separating distance between pads is requested to be as small as the size of the object to be connected. This challenge opens a research field that could be named "packaging for nano-devices," which can take benefit from the solutions developed both in the classical packaging field and the 3D integration field. Some nano-devices, such as atomic wires for instance, indeed require a specific receiving surface (addressed by the packaging field through the development of surface treatments), which implies vertical electrical connections to avoid its damaging (connections addressed by the 3D integration field through the development of vias or TSV). One of the main challenges is then to achieve the fabrication of two nanoscale vias (later referred to as nanovias) separated by the smallest possible distance, meaning in the order of magnitude of a few tens of nanometers. The nano-object is connected to nanovias thanks to nanopads which are processed on the receiving surface. A technology based upon the nanovias implementation with a Focused Ion Beam (FIB) has already been explored [21, 22]. The step beyond such a technology is to develop a compatible capping to protect the nano-device; this is under development at CEA-LETI, and the first results will be presented in this paper.

First, the technological process flow necessary to develop this kind of chip will be described. The FIB-based processes required for the nanovia fabrication will be presented, and their influence on nanovia morphology will be detailed. Then, nanopads process will be investigated both by simulation and experiment. Lastly, the first integration of a reconstructed substrate equipped with nanopads and protected with a cap substrate will be presented.

2 Specifications for Atomic-Scale Device Packaging

The problem to solve will be clearly understood by referring to Fig. 1.

This figure describes a die comprising an atomic-scale device, such as a molecule, on the front side of a Silicon-On-Insulator substrate (SOI), and protected with a hermetically bonded silicon cap. This cap is equipped with a cavity (corresponding to the atomic-scale device) and lateral bevels to facilitate its release. The atomic-scale device is connected to nanopads consisting in implanted areas in the silicon layer of the SOI substrate. These ones are linked to nanovias etched through a membrane previously prepared on the backside of the SOI substrate.

The fabrication of the atomic-scale device needs a perfectly ordered surface to avoid any variability. Perfect surface size specification is about 100 × 100 nm^2 which requests the surface to present terraces with a similar size. The surface is thus reorganized according to a Si(001)-(2 × 1):H structure [23] obtained with a smoothing treatment carried out under hydrogen at high temperature (between 950 and 1100 °C) [24]. Such H-passivated surface is not very stable at ambient atmosphere and consequently requires a temporary protection. It has been achieved through the addition of a temporary cap substrate. The debonding ability of this cap is ensured by a low-energy direct hydrophobic bonding process. This protection step however severely limits further thermal treatments, as the bonding energy is strongly reinforced with temperature. Surface smoothing and protection are consequently performed at the end of the integration process. The corresponding process flow is presented on Fig. 2.

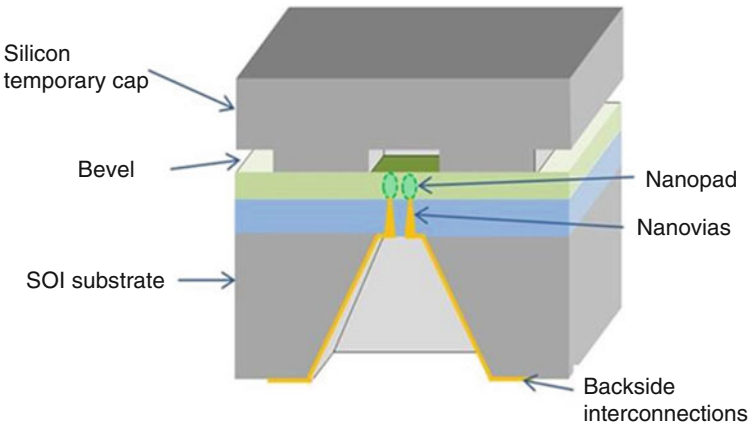

Fig. 1 Drawing of a chip connecting a molecule, a nano-object, or an atomic-scale circuit. The electrical interconnection comprises (i) nanopads to which the molecule is connected, (ii) nanovias achieved with a FIB tool through a membrane delimiting one wall of the cavity, and (iii) backside lines and contacts. *Gray* and *green* parts correspond to silicon, whereas the *blue* part is silicon oxide

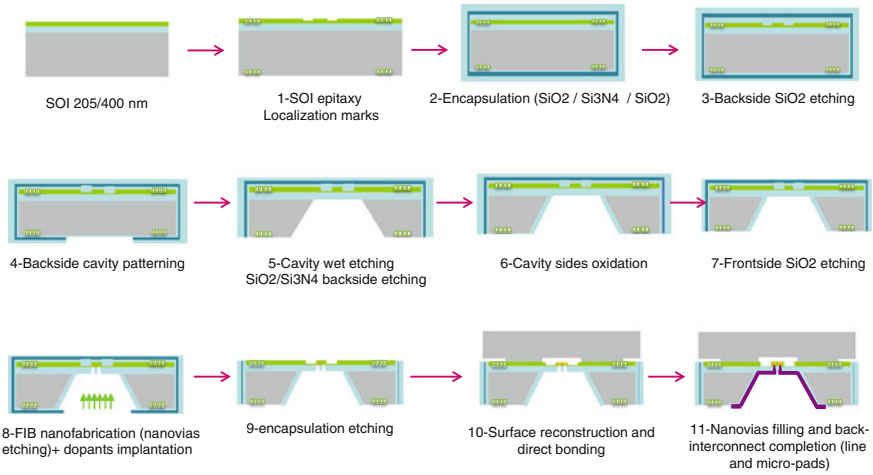

Fig. 2 Details of the process flow enabling the fabrication of a nanoscale device packaging

This flow includes 11 technological steps:

Step 1: Fabrication of localization marks in order to be able to identify the area of interest and to localize the nanopads during the nano-object positioning (where the atomic-scale device is achieved).
Step 2: Encapsulation of the substrate with a $SiO_2/Si_3N_4/SiO_2$ tri-layer mask in order to protect the wafer during the backside cavity deep etching.
Steps 3 and 4: Hard mask patterning for cavity etching.
Step 5: Cavity wet etching (until the buried oxide layer (BOX)).
Step 6 and 7: Cavity walls oxidation and front side SiO_2 etching.
Step 8: Nanovias etching in a FIB tool and dopant implantation through the nanovias (nanopads fabrication).
Step 9: Encapsulation layers removal.
Step 10: Surface reconstruction and bonding of a temporary protection. In the meantime, doping species are activated.
Step 11: Nanovias filling and backside interconnections achievement.

According to this flow, one can distinguish four major and challenging modules which are steps 5, 8, 10, and 11. Once this die has been obtained, three main additional steps need to be validated and concern the cap release, the atomic-scale device construction, and the final hermetic capping at a temperature that does not damage the device. This paper will focus on the major modules 5, 8, and 11, related to the fabrication of the nano–micro connecting path (nanopads, nanovias, and the backside interconnection, at the bottom of the backside cavity). The surface module (step 10) has already been investigated, and the published results will be reminded at the beginning of the next chapter.

3 Technological Steps

3.1 Surface Smoothing and Temporary Protection

Silicon surface smoothing is a prerequisite for STM-based atomic-scale device design as a perfectly ordered surface is needed. This process is carried out at wafer scale in a Reduced Pressure–Chemical Vapor Deposition (RP-CVD) reactor at high temperature (950–1100 °C) and leads to a perfectly ordered hydrophobic Si(001)-(2 × 1):H surface [25]. This H-passivated surface is not stable and needs to be protected with a removable cap. Among the possible bonding solutions [24], silicon direct bonding appears as the most relevant option:(i) The bonding process can take advantage of hydrophobic smoothed surface. (ii) Such a bonding is characterized by a low-energy interface, which is strengthened with a temperature as high as 400 °C, below this temperature, the substrates can be debonded, which makes this bonding process compatible with a temporary capping [26]. (iii) Such a bonding does not require any material addition and is suitable with an Ultra-High Vacuum (UHV) process. Moreover, since the post-processing steps beyond those described on Fig. 2 will be achieved in an Ultra-High Vacuum chamber, only samples with a size of 1 × 1 cm^2 are envisioned. This adds another constraint which concerns the capability for the assembly to be diced into samples, meaning that bonding energy must be high enough to undergo the dicing step without any separation of the wafers.

3.2 Nanoscale Via Achievement by FIB

3.2.1 Backside Deep Cavity Processing

Prior to the fabrication of the connecting path, a cavity as deep as the substrate thickness is etched on the wafer backside. A classical wet anisotropic etching of silicon is carried out with a Tetra-Methyl Ammonium Hydroxide (TMAH) solution. Three square cavity sizes of 1.2, 1.4, and 1.6 mm, respectively, have been chosen (R, S, T notations on Fig. 3). They have been calculated in order to get a bottom surface which edge is about a few hundreds of microns. Regarding the depth of the cavity, etching process duration is about 20 h, meaning that the substrate had to be specifically protected to undergo such an etching duration. When the chip substrate is a SOI substrate, the buried oxide layer is used as an etch stop layer, but care must be taken to avoid any attack of this layer. The SOI characteristics are given as follows: Si 200 nm/Box 400 nm/Si 725 µm. Figure 3 illustrates different cavities obtained on a 725-µm-thick bulk Si substrate (upper images) and a SOI substrate (lower images).

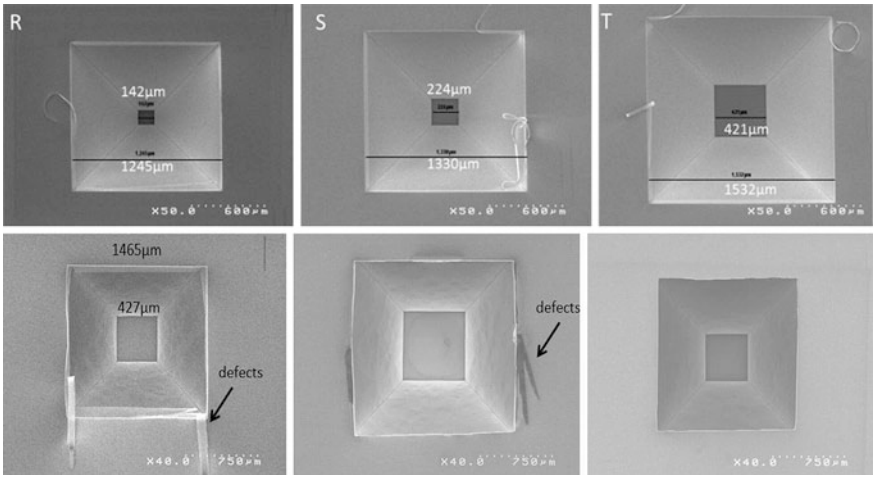

Fig. 3 SEM pictures showing the three cavity sizes after etching on the backside of the silicon substrate and defects removal (*Upper images* silicon bulk substrate, *lower images* SOI substrate)

During this step, defects have been observed due to the deep TMAH lateral over-etching. A specific chemical wet cleaning has been developed, and the defects have successfully been removed.

An optical microscope control conducted on the front side SOI substrate after cavity etching is shown on Fig. 4 and demonstrates that the localization marks processed during step 1 can be successfully identified at the center of the membrane.

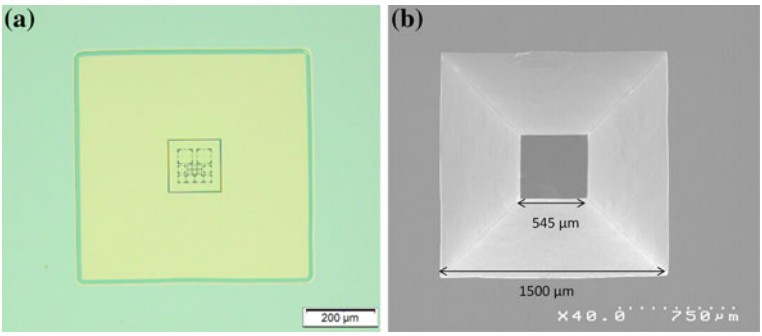

Fig. 4 **a** Frontside optical microscope picture of a 600 nm-thick membrane. **b** SEM observation of the backside deep cavity

3.2.2 FIB Tools

Nanovias are fabricated with a FIB tool. The gallium beam enables nanovias etching and filling through the decomposition of a tungsten-based precursor ($W(CO)_6$). The nanovias fabrication process has been developed in two different tools. The first one is a sample-scale FIB where process is developed on a 1-cm^2 sample, whereas the second one is a wafer-scale FIB set in a clean room and operating on 200-mm silicon wafers.

The development of nanovias fabrication processes has first been conducted on Si samples covered with a 400-nm-thick SiO_2 layer, mimicking the future SOI substrates used in the final integration flow. The first work has consisted in the control of (i) the nanovia etching stop (at the SiO_2/Si interface), (ii) the nanovia geometry, and (iii) the nanovia filling. The second step has consisted in studying the impact of the nanovia fabrication process on the surface reconstruction process and on the final surface quality. The process has finally been transferred at the wafer scale on SOI substrate.

3.2.3 Development of the Nanovia Etching and Filling Processes

In the sample-scale FIB equipment used for the first developments, etching stop has been accurately controlled by monitoring the transmitted current through the Si substrate (accuracy of 5 %), and after further optimization of etching and filling parameters, a well-controlled etching stop at the SiO_2/Si interface and a void less filling have been obtained.

When transferring the processes toward a wafer-scale FIB tool, equipped with a detector set farther from the substrate, this method for controlling the etching stop could not be used anymore: nanovias have thus begun to be etched and filled while monitoring the process duration, which requires to adjust etching and filling parameters at the beginning of each experiment to gain accuracy. Etching takes 2 s on average for a 100-nm-diameter nanovia, whereas filling takes between 3 and 8 s.

Regarding nanovia filling, the main difficulty lies in the control of the over-etching as both etching and filling phenomena are co-existing during the filling step. Further optimization on both etching and filling parameters has conducted to voidless nanovias. Nanovias with a geometry of 100 nm in diameter and 400 nm high have been obtained with a good reproducibility. These results are illustrated on Fig. 5.

The use of a gallium beam for the nanovias fabrication raises the question of the management of non-intentionally implanted gallium atoms in the SOI film, and especially as gallium has a low melting point (30 °C), whereas a surface reconstruction process at high temperature (950–1100 °C) ends the integration flow. A study on the impact of the nanovia fabrication process on the surface reconstruction process and on the final surface quality has thus been launched. Three types of nanovias have been fabricated and characterized, in order to simulate the three technological steps at stake: (i) etched nanovias, (ii) etched and thermally treated nanovias (simulation of the surface reconstruction step), and (iii) etched,

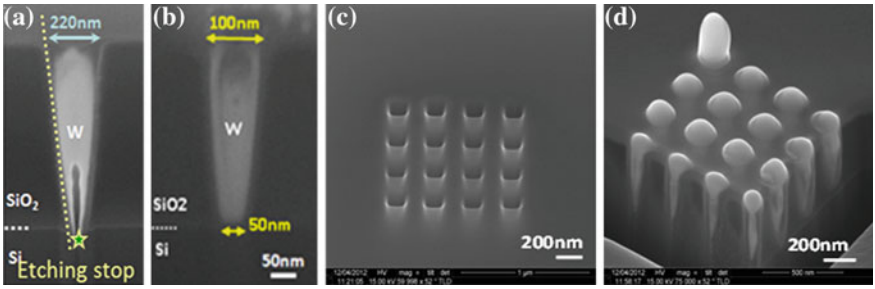

Fig. 5 Nanovia with a 100 nm diameter and a 400 nm height **a** before etching-stop optimization, **b** after etching stop, filling, and geometry optimization, **c** 4 × 4 nanovias matrix after SiO_2 etching, **d** 4 × 4 nanovias matrix after W filling

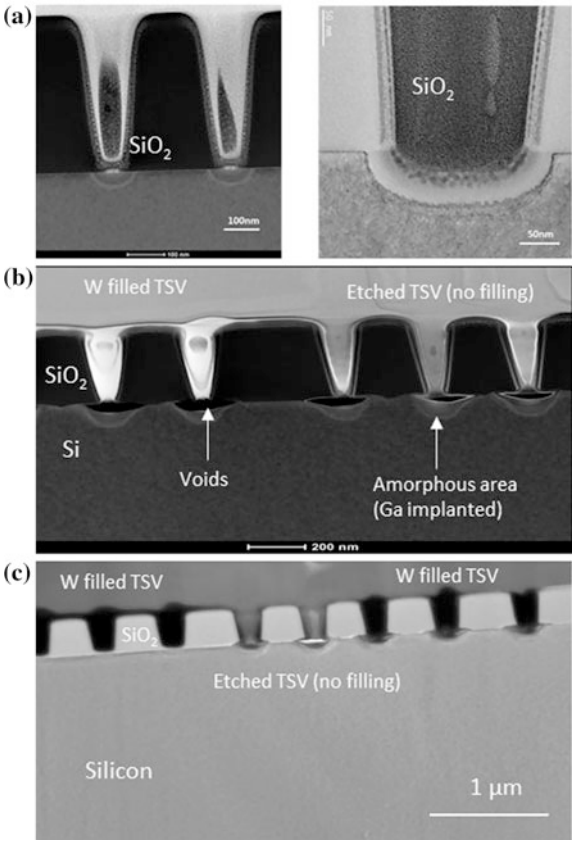

Fig. 6 TEM analysis of nanovias. **a** 100 nm nanovias after the etching step, **b** etched and thermally treated nanovias (100 nm in diameter), some of them being moreover filled, **c** etched and thermally treated nanovias (200 nm in diameter), some of them being moreover filled

thermally treated, and filled nanovias (corresponding to the final step of the integration process). Results are illustrated on Fig. 6.

Voids and amorphous areas have been observed at the bottom of some nanovias. On Fig. 6a, an amorphous layer of 50 nm can be observed at the bottom of the nanovia. It can be explained by a high gallium beam current which at least produces a gallium ion implantation in the silicon film and which can result in an amorphous SOI layer. Voids have been observed at the bottom of nanovias after thermal treatment. All the interactions between gallium atoms, cleaning solutions, and thermal treatment have not totally been understood yet and are still under investigation. However, it has been noted that etching stop plays an important role, and it seems that an etching stop in the SiO_2 layer could prevent the apparition of void at the SiO_2/Si interface after surface reconstruction, as it can be seen on Fig. 6c on the nanovias on the left side of the image. This hypothesis has been the object of a specific study as illustrated on Fig. 7.

Compared to the previous study, an arsenic implantation of the SOI film has been conducted through the 200 nm-diameter nanovias and the dopants have been activated during the thermal treatment at 950 °C. The two configurations, etching stop at the SiO_2/Si interface and etching stop in the SiO_2 layer, are presented on the TEM picture on Fig. 7. The etching stop and the tungsten filling at the SiO_2/Si interface have modified the nanovias geometry (Fig. 7a). The nanovia geometry has been preserved when the etching stop has been achieved in the oxide layer, located several nanometers above the Si/SiO_2 interface. The oxide layer at the bottom of the nanovia has protected the silicon surface, and the voids previously observed have not been detected. The connection between the nanopads and the nanovias has been completed with a wet chemical etching containing hydrofluoric acid (Fig. 7b). With this protocol, the amorphous area has been recrystallized during the surface reconstruction process. However, dislocations have been observed in both cases, which leads to the conclusion that these defects have been generated by arsenic implantation at high energy (150 keV).

Figure 8 provides a chemical analysis of the 200 nm-diameter nanovias. It should be noted that the EDX sensitivity is ~0.5 wt% for a given element, which means that the amount of implanted gallium is greater than this detection limit.

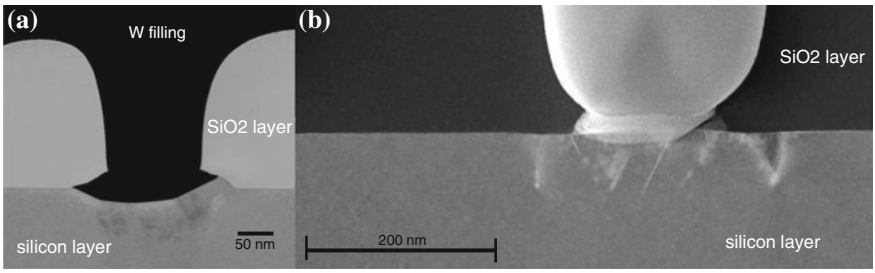

Fig. 7 TEM picture of 200 nm nanovias, after nanovias etching, arsenic implantation, thermal treatment at 950 °C, and tungsten filling. **a** Nanovias with etching stop at the SiO_2/Si interface, **b** Nanovias with etching stop in the SiO_2 layer

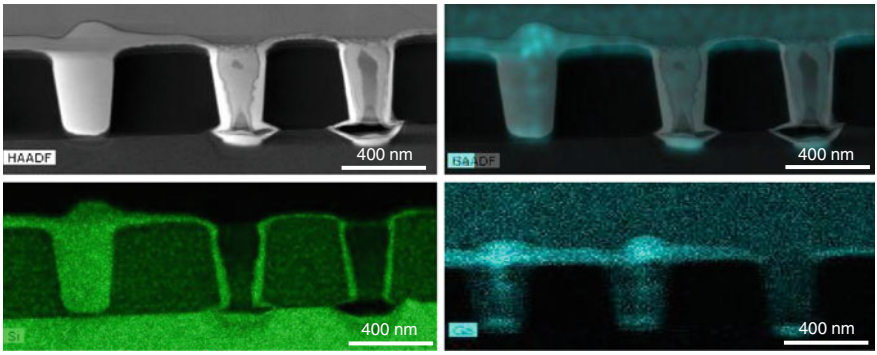

Fig. 8 EDX analysis of 200 nm nanovias showing the Si distribution (image on the *bottom left*) and the Ga distribution (image on the *bottom right*). The STEM image is shown on the *top left*, whereas the image on the *top right* results from the superposition of the STEM and EDX-Ga images. Scale bar is 400 nm

Observations on etched nanovias (Fig. 6a) have clearly put forward the presence of a 50 nm-thick amorphous layer at the bottom of etched nanovias. This layer has been identified as a Ga-implanted layer with EDX analysis. Considering now etched and thermally treated nanovias (Fig. 6b), a defective area corresponding to a Ga-implanted region, as evidenced by EDX analysis, is still observed at the bottom of both open and blind nanovias and extends over a thickness of $\sim$200 nm for open nanovias, while it extends over $\sim$50 nm for blind nanovias (as for etched ones). In this late case, the defective area seems to be crystalline, whereas it appears partially amorphous in the case of open nanovias. This is a key point to be taken into account for the future work on the whole integration, as this defective area is in the same order of magnitude as the thickness of the Si film of SOI substrates for open nanovia, whereas it is smaller and becomes crystalline for blind nanovias after thermal treatment. Moreover, unexpected voids have been observed at the extremity of open nanovias, whether they are empty or filled. Such voids have not been observed in the case of blind nanovias and have been specifically observed after thermal treatment (surface reconstruction): no such voids have been observed on etched nanovias. One possible explanation for the presence of such voids could be related to the chemical solutions used in the cleaning step prior to the thermal treatment at 950 °C: assuming the observed voids indeed correspond to a Ga-rich area prior to surface cleaning, this Ga-rich amorphous material may have been etched during surface cleaning. This assumption has however to be further investigated with additional experiments.

Electrical properties of such FIB-fabricated nanovias have furthermore been explored. First, regarding the characterization of the filling material, the electrical resistance of the deposited tungsten has been measured on an appropriate structure

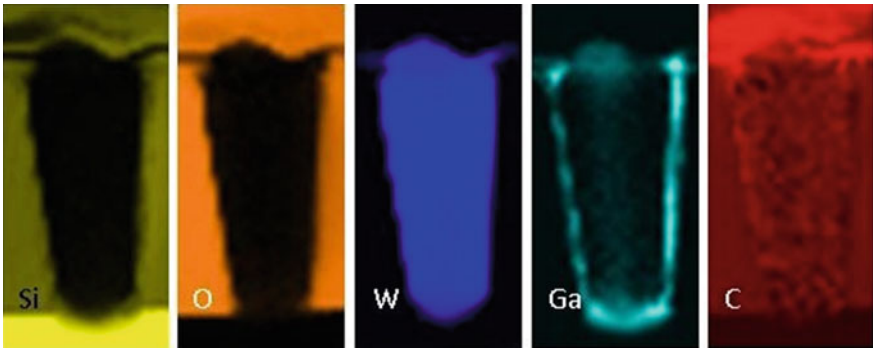

Fig. 9 EDX analysis of etched and filled nanovia of 150 nm diameter: chemical distribution of Si, O, W, Ga, and C

and the experimental material resistivity has been found to be two orders of magnitude higher than for the bulk material (experimental value: 2.4×10^{-6} Ω m). This can be explained by the partial dissociation of the $W(CO)_6$ gas under the ion beam, which has been confirmed by the EDX analysis of the nanovia composition (Fig. 9): tungsten has been found as the major element (75 mass%); carbon (10 mass%), oxygen (5 mass%), and Ga traces have also been found. Moreover, there is no composition variation with deposition time leading to a homogeneous material composition over the whole nanovia.

Electrical characterization of the nanovias has been tested through Scanning Spreading Resistance Microscopy (SSRM), which is a probing technique using an AFM in contact mode with a conductive tip. These tests aimed at evidencing conductive areas (W-filled nanovia) in the insulating substrate (SiO_2), and at trying to extract nanovias resistance. Nanovias have been successfully evidenced (Fig. 10), but their resistance could not be extracted as it has been found negligible compared to the access resistances. However, a resistance variation over 2 orders of magnitude has been measured between the substrate and the nanovias.

Beside the understanding of the interactions between the etching, filling, and reconstruction processes at the bottom of nanovias, the integration technology has been developed and these processes have been implemented at the wafer scale. Matrices of nanovias have been successfully FIB-etched and filled at the bottom of 480 µm-deep cavities (Fig. 11).

The nanoscale/microscale connection between nanovias and contact pads has been completed through the deposition of tungsten lines along the cavity side, using the same wafer-scale FIB. A continuous electrical path has thus morphologically been demonstrated, on the substrate backside, from nanovias to electrical contact pads (Fig. 12).

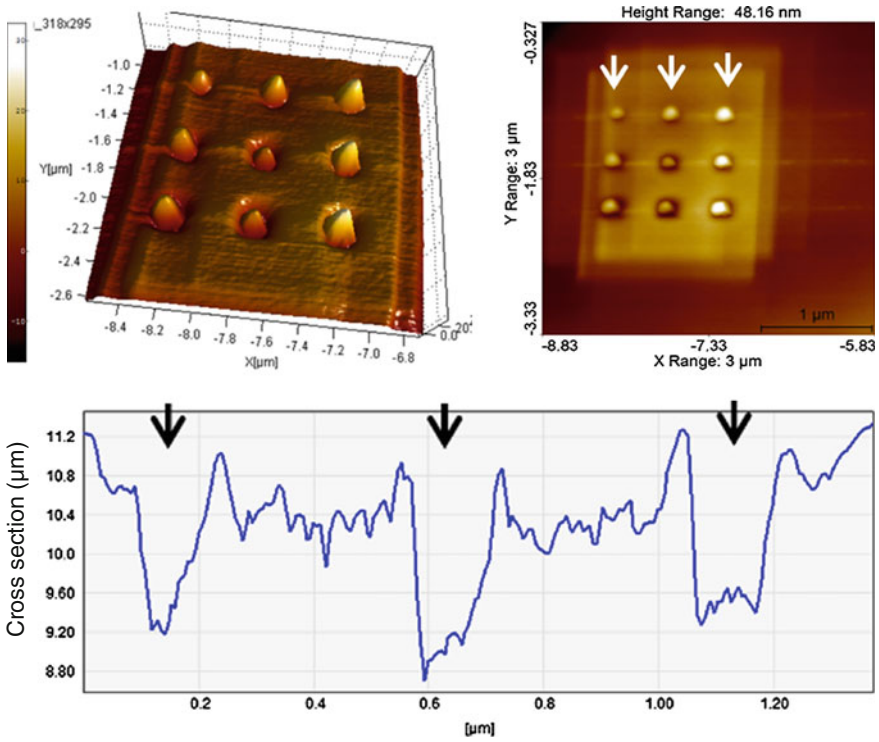

Fig. 10 SSRM results. Maps showing resistance variation over a matrix of 3 × 3 nanovias and graph showing the variation of Log R as a function of the scanning distance (µm) (1st matrix line)

3.3 Nanopads Processing

Implanted areas (referred to as nanopads) ensure the electrical continuity between the molecular/atomic circuit on the top surface and the nanovias. Nanopads are fabricated by implanting dopants on the SOI film, from the substrate backside, through FIB-etched nanovias (Fig. 2, step 8). Dopants are activated during surface reconstruction: the thermal budget of this step is however higher than required for dopants activation and diffusion is expected to occur, which implies the nanopads enlargement and possible short-circuit. Two main issues have been addressed:

- Nanopads spreading during the surface reconstruction process: this point has been investigated by calculation and measurements after dopants diffusion;
- Impact of doped areas on the surface reconstruction.

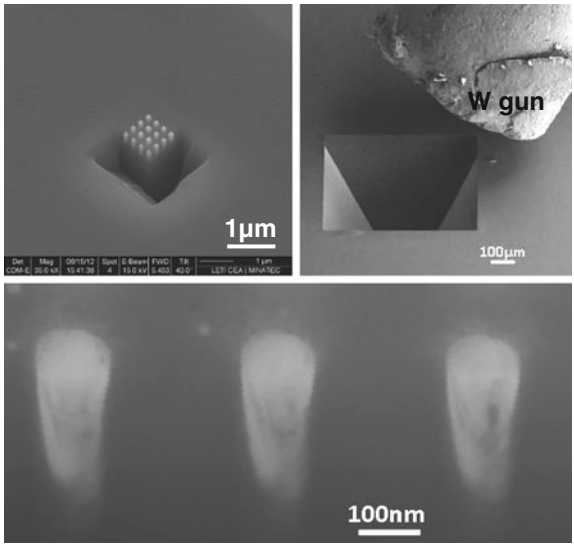

Fig. 11 4 × 4 matrix of 100 nm nanovias at the bottom of a 480 µm-deep cavity

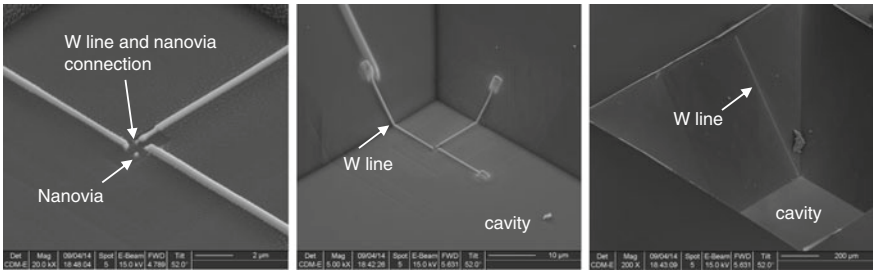

Fig. 12 SEM picture of nanovias, metal line in the bottom of the cavity, and backside-interconnect completion on SOI substrate (*Right figure* is an enlarged view of *left figure*)

3.3.1 Interconnection Resistance Calculation

Dopants diffusion has been simulated, and the expected resistance of the interconnection system has been estimated. Simulation has been performed with the S-Process software (Synopsys). Two doping species have been taken into account: arsenic, which creates a lot of crystal defects when implanted, and phosphorous, which generates a lower defectivity but has a higher diffusivity in silicon than arsenic. The implantation conditions are described in Table 1.

These implantation conditions have been chosen in order to ensure the highest doping level for the nanopads (in order to minimize their electrical resistance), while still enabling the reconstruction of the damaged layer. For this latter point, the implantation energy has been chosen so as to leave a crystal seed of a few tens of

Table 1 Energy and dose parameters used for an implantation in a 200 nm-thick silicon layer

Dopants	Implantation energy	Implantation dose
Arsenic	145 keV	5E15 at./cm^2
Phosphorous	90 keV	3E15 at./cm^2

nanometers. Monte Carlo simulations have been run and show that the Si film is expected to become amorphous on 180 nm thick after implantation, which lets 20 nm of crystalline silicon to enable the film reconstruction (Fig. 13).

A reconstruction process at 950 °C (rather than the 1100 °C classical process) has been considered in order to reduce dopants diffusion while still enabling surface reconstruction. Several geometries (diameter, spacing) and implantation conditions have been tested, in order to (i) get the smallest gap between nanopads after surface reconstruction while avoiding short-circuit, (ii) get the highest doping level (lowest resistance) while not damaging the surface (i.e., avoiding an amorphous surface).

Process simulations indeed show that the thermal budget used for a surface reconstruction at 950 °C is affordable from nanopads view, adapting nanovias geometry and dopant type. In the case of an As implantation through nanovias of 100 nm in diameter and spaced of 350 nm, the distance between nanopads after diffusion during 12 min at 950 °C is expected to be 125 nm (Fig. 14a), and the doping concentration on the frontside is expected to be about 8×10^{18} at. cm^{-3} (Fig. 14b). Moreover, the surface treatment process duration does not show a great difference between 6 and 12 min.

The expected resistance of nanovias and nanopads has been calculated, and the results are shown on Fig. 15. It takes into account a nanovia filling with tungsten. A resistance in the range of a few hundreds of ohms is expected. It should be noted that contact resistances have not been considered in this calculation.

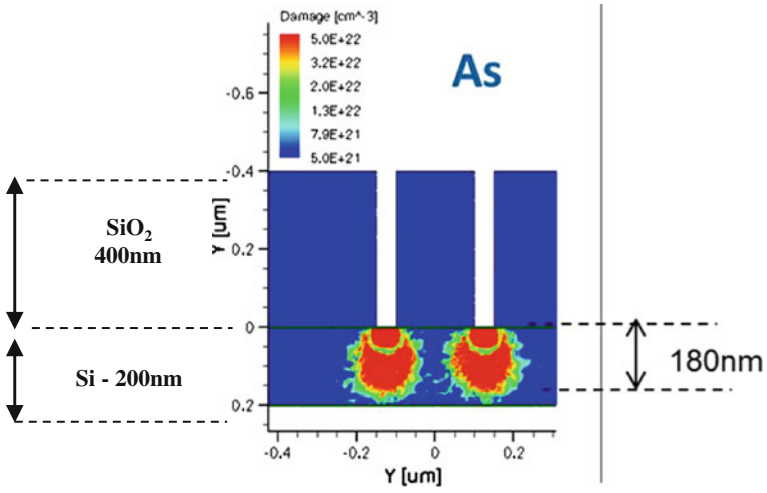

Fig. 13 Illustration of a Monte Carlo simulation result obtained on arsenic: simulation shows the amorphous area (~20 nm crystalline silicon remaining). Damage concentration scale is graduated from *blue* (5×10^{21} cm^{-3}) to *red* (5×10^{22} cm^{-3})

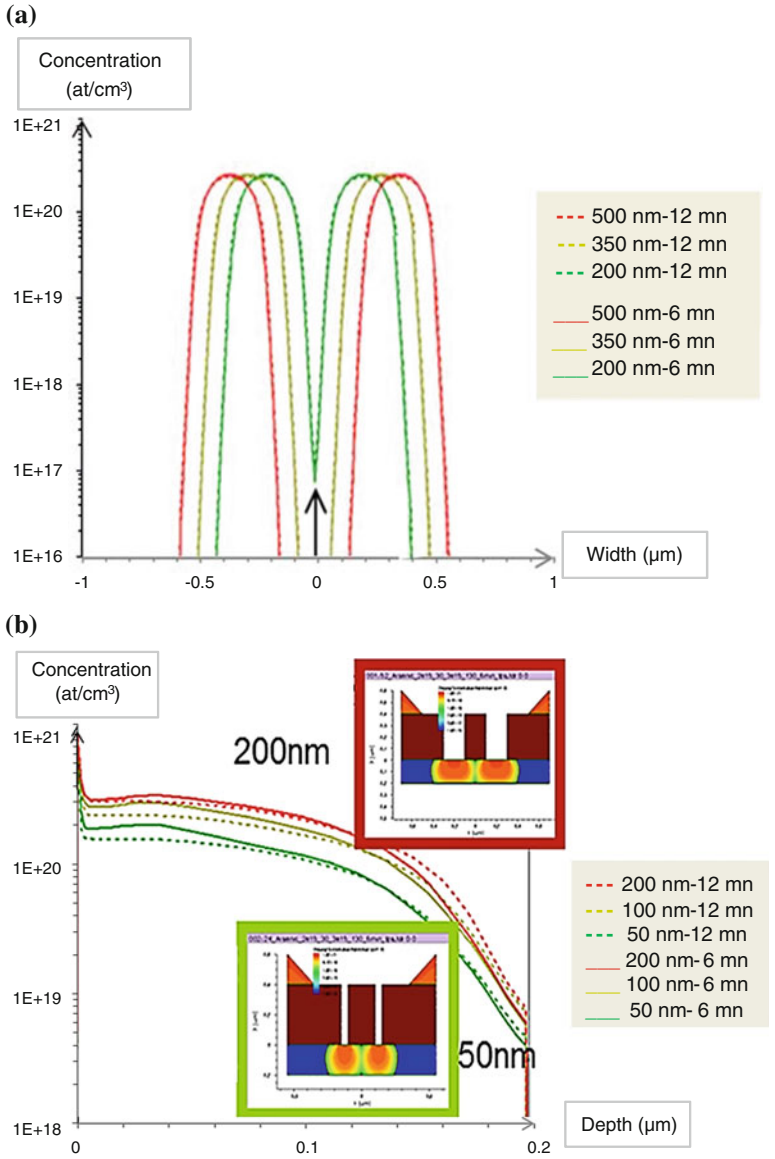

Fig. 14 Illustration of a simulation result obtained for As: **a** concentration versus width for 100 nm diameter nanovia, **b** doping profiles obtained for various nanovia diameters

Besides, it should be kept in mind that the standard Si substrate resistivity is in the order of 1–50 × 10^4 Ω μm, namely 25 kΩ–1.25 MΩ for a space of 100 nm between nanovias. This means that the resistance of the Si film might be in the same order of magnitude as the resistance of the molecule/atomic circuit. A way for

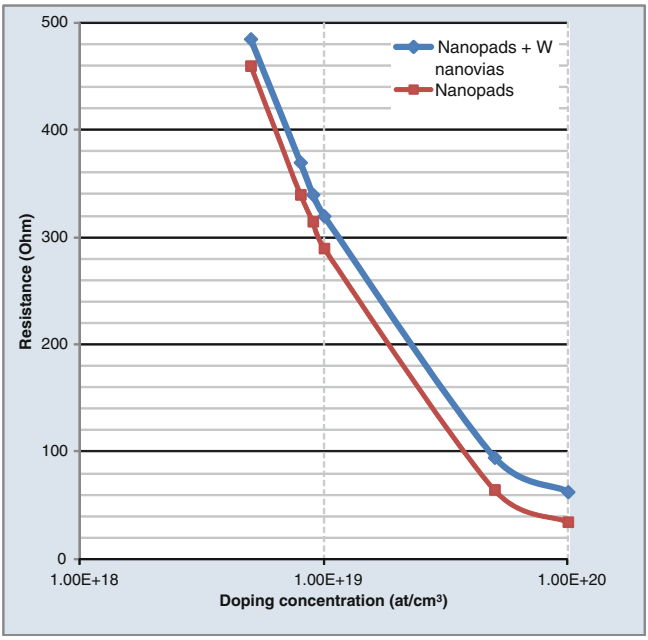

Fig. 15 Calculated resistance of the nanopads and nanovias. Nanopads of 200 nm in a 200 nm-thick Si film, and nanovias of 200 nm in diameter in a 400 nm-thick oxide layer have been considered for this calculation

solving this problem could be to implement this technology on high silicon resistivity substrates (>10^6 Ω μm).

3.3.2 Nanopad Design

Based on these simulation results, two sets of e-beam lithography masks, namely A and B, have been designed: the mask A aims at evaluating the impact of nanovias fabrication and dopants implantation on the surface properties. It consists in nanopads matrices, with varying diameter, space, and density (Fig. 16a). The mask B intends to evaluate dopants diffusion during surface reconstruction and to measure leakage currents, in order to control the distance between nanopads. It consists in circular patterns of 300 μm in diameter, containing radial lines of either 50 nm or 100 nm wide. This design is more dedicated to SSRM and STM studies (Fig. 16b). Both series of masks are equipped with specific patterns to locate implanted areas.

These two e-beam masks include different nanopads designs, such as (i) the number of implanted pads in the circular patterns, (ii) the doped pads width, and (iii) the distance between the nanopads. Table 2 describes the mask B patterns and geometries (Fig. 16b).

Figure 16 illustrates the above-mentioned designs implemented on a stack composed of: 400 nm thick of e-beam photoresist/400 nm thick of SiO_2 layer/silicon substrate. Figure 17a–e respectively correspond to the designs of Fig. 16a, b.

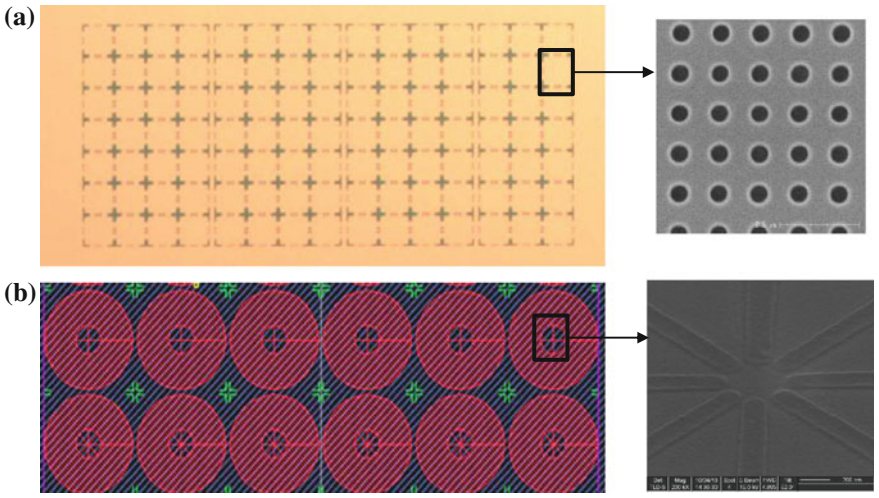

Fig. 16 Two e-beam masks designed: **a** mask A is dedicated to the study of the impact of nanopads on the surface reconstruction, **b** mask B is dedicated to the study of dopants distribution after diffusion during surface reconstruction

Table 2 Design variations for the mask B: the distance between the doped lines varies between 100 nm and 400 nm, while their width is either 50 nm or 100 nm. A pattern features 2, 4 or 8 such lines

Implanted lines number	Distance between implanted lines				
	100 nm	200 nm	250 nm	300 nm	400 nm
2 lines	Implanted line width: 50 and 100 nm				
4 lines					
8 lines					

A preliminary surface investigation has been conducted on the sample corresponding of the mask A (Fig. 16a) after photo-resist removal. This experiment has been achieved with an AFM tip (tapping mode). A matrix of 7 × 7 nanopads has been implanted in 12 μm^2, thus demonstrating an interconnection density as high as $4 \times 10^6/mm^2$. Such a structure is shown on Fig. 18.

In the same way, dopants distribution has been investigated after thermal treatment and diffusion at 950 °C with Scanning Capacitance Measurement (SCM). This technique gives a direct correlation between capacitance and dopants concentration. An electrical modulation is applied on the sample, and the capacitance variation correlates to the dopant type. SCM characterization has been conducted on the implanted lines (mask B (Fig. 16b)) with the conditions described in Table 2. Figure 19 illustrates such measurements on a four implanted lines configuration: the yellow part corresponds to the P-doped silicon substrate, while the blue part represents the N-doped areas. This experiment has enabled the measurement of the diffusion length with the distance defined in the mask (before diffusion) as

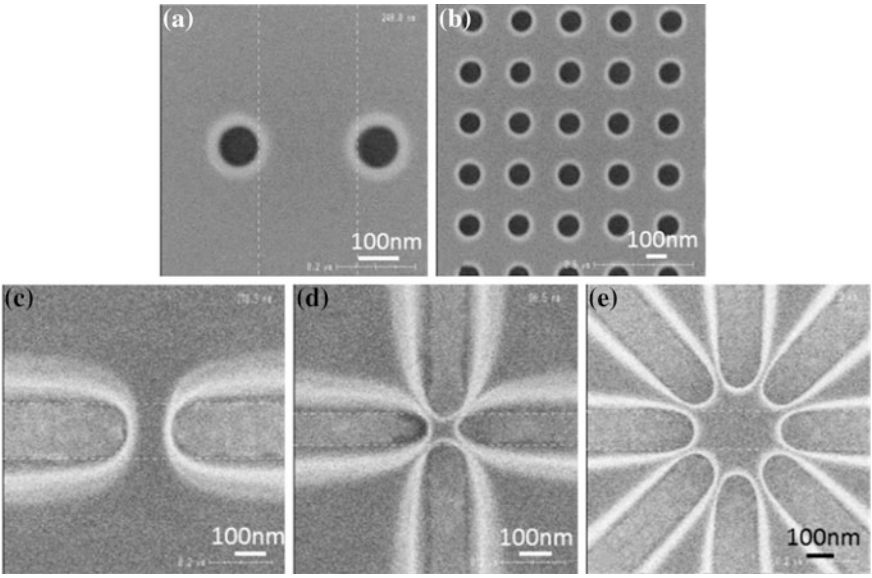

Fig. 17 SEM observations of nanopads after e-beam lithography. **a** 2 isolated nanopads (mask A); **b** matrix of nanopads (mask A); **c**, **d**, **e** implanted lines delimiting nanopad geometry (mask B)

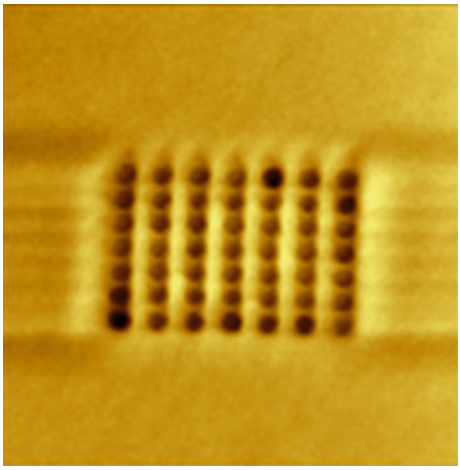

Fig. 18 AFM picture obtained in tapping mode imaging a 7 × 7 matrix of arsenic-implanted nanopads

reference. Figure 19a has demonstrated that a short-circuit is experimentally observed with a distance designed at 200 nm. Using a distance of 250 nm between the four electrodes (Fig. 19b), an edge side short-circuit has also been noticed. Regarding the distance of 350 nm between the 4 electrodes (Fig. 19c), no

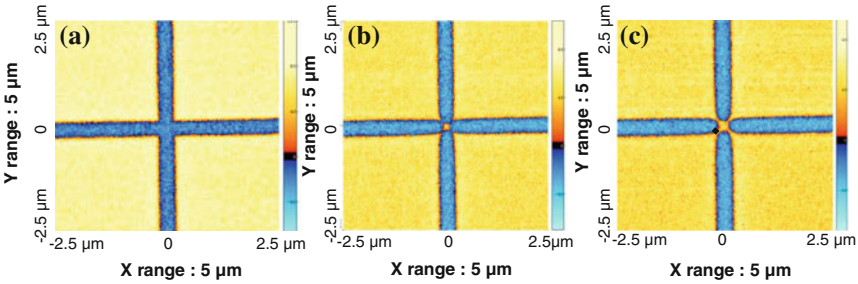

Fig. 19 Scanning Capacitance Measurement (SCM) pictures with different spacing between four electrodes after surface smoothing at 950 °C. **a** Short-circuit is observed with a 200 nm distance, **b** an edge side short-circuit is observed with a 250 nm distance, **c** no short-circuit is observed with a distance of 350 nm initially designed

short-circuit between implanted lines has been observed and the distance measured between neighbor's electrodes after diffusion is 60 nm. This experimental value is in agreement with the distance reported in the simulation after dopants diffusion (125 nm) (Fig. 14a), though it is a bit lower than expected. These first results meet the requirements of STM-based atomic-scale wires and let think that a nano-objet could be deposited and connected between the implanted lines.

3.3.3 Nanopads Impact on Surface Reconstruction and Bonding

A study has been conducted to determine the effect of surface implantation on the bonding quality. The SOI substrate has been implanted according to the nanopads design, and its surface has been reconstructed. Finally, this SOI substrate has been capped with a surface-reconstructed silicon wafer. The fabrication of such a test vehicle has required (i) the fabrication of localization marks intended to ease the finding of nanopads during the characterization phase; (ii) the development of e-beam lithography which has been a challenging part because of the wide range of patterns studied and the thick resist used (400 nm) for implantation; (iii) the implantation of nanopads, using the simulated conditions; and (iv) the surface preparation (cleaning, surface reconstruction at 950 °C), the surface preservation with the hydrophobic bonding of a patterned cap wafer, and dicing. A Scanning Acoustic Microscope (SAM) picture of this test vehicle before dicing is shown on Fig. 20. Bonding defects are put forward (white parts) and appear most of the time on the patterned parts of the substrates corresponding either to implanted areas for the bottom substrate, or to etched bevels for the top one.

A scanning Tunneling Microscopy (STM) characterization has been conducted on the P-implanted samples in order to image the doped surface after reconstruction. The characterizations have been carried out in an Ultra-High Vacuum (UHV) system with a base pressure of 5×10^{-11} mbar. The Low-Temperature STM (LT-STM) measurements have been performed at 4 K with electrochemically etched polycrystalline tungsten tips used as probes. The debonding step has been

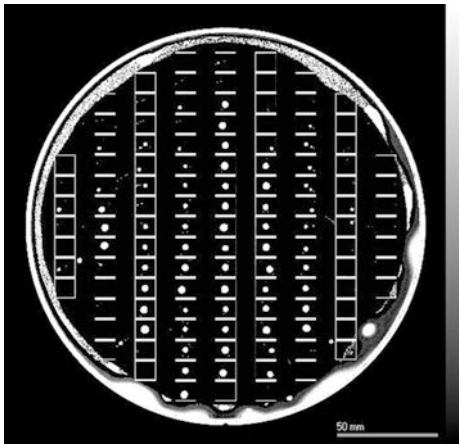

Fig. 20 Scanning Acoustic Microscope (SAM) picture of bonded wafers (200 mm SOI substrate with implanted nanopads and Si cap with etched bevels)

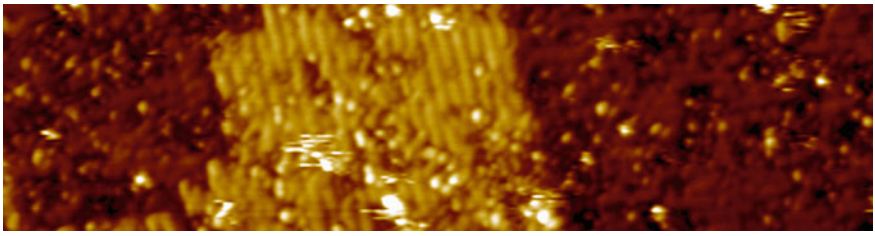

Fig. 21 LT STM image (V_{bias} = −2 V and I = 10 ρA) of the Si(001):H surface. The H-Si dimer rows are locally observed

successfully achieved in the UHV equipment, validating the temporary silicon cap protection concept. Immediately after their debonding, the P-doped samples have been transferred to the cryostat, where they have been cooled down to 4 K. Because of the samples surface preservation with a bonded cap, no additional surface preparation has been applied.

The SiH(001) surface with P-doped Si areas has been investigated, and the result is presented on Fig. 21.

The observation of dimers rows demonstrates that the implanted regions have been correctly rebuilt during the surface reconstruction treatment at 950 °C. However, the surface quality of the P-doped sample is lower than for undoped samples and surface defects have been observed. Surface disorder may indeed have occured during the fabrication of localization marks or during implantation. Although this process requires improvements, it shows that an implanted surface can be properly reconstructed by a surface treatment and it emphasizes the great potential of this technology for the future production of functional electronic devices at the nanoscale.

4 Summary and Conclusion

A new technological field for the packaging of atomic-scale devices on 200 mm SOI substrates has been opened. This technology includes both surface reconstruction and capping, and electrical interconnection developments. The technological developments of the required modules have been described before their integration in a complete process flow. Due to the first requirements on the surface quality, silicon direct bonding has been identified as a suitable technology for the preservation of silicon wafers that have undergone a smoothing surface treatment. This packaging technology is reversible, meaning that it is possible to temporarily protect the device and is strong enough to allow the substrate dicing into chips. The second requirement concerns the interconnections between the atomic-scale circuit and external connection pads. This interconnection is composed of nanopads made of silicon-doped zones in the silicon part of the SOI wafer, connected to nanovias, fabricated in a FIB tool through the oxide layer of the SOI. Prior to the interconnections achievement, a deep cavity has been patterned in the backside of the wafer down to the oxide layer, in order to drill the nanovias. This deep cavity leaves a 600 nm-thick membrane on which the atomic circuit will further be achieved. The interconnection completion, from nanovias to electrical contact pads, has been ensured by tungsten lines deposited by FIB at the bottom of the cavity, and along the cavity sides. The connection between the nanopads (nanometric scale) and the electrical pads on the wafer backside (micrometric scale) has been correctly achieved.

The presented technology relies upon the fabrication of nanovias with a FIB equipment. 100 nm and 200 nm-diameter nanovias have been successfully etched and filled. TEM observations of nanovias have shown an amorphous Ga-implanted area in the silicon part: this layer has been chemically and structurally investigated, and further studies are now needed to achieve the control of this Ga-rich area. Regarding nanovias filling process, it has been achieved with FIB-deposited tungsten which shows a resistivity two orders of magnitude higher than the bulk metal. Electrical measurements performed on a 3×3 nanovias matrix have demonstrated that nanovias were clearly insulated from each other's. The distance between two [nanovias + nanopads] has been simulated and measured by SCM and has demonstrated that the lowest distance separating two 100 nm diameter nanovias was 60 nm. This is in the same order of magnitude as a STM atomic-scale wire. Finally, a substrate equipped with implanted nanopads has been reconstructed and bonded. The observation of this first assembly has not revealed any bonding defect except in the doped or etched parts of the substrate. STM has demonstrated that the reconstruction process at 950 °C was able to rebuilt the amorphous areas created by the deep implantation and has evidenced Si:H dimers on the surface.

Further investigations will be conducted on the surface reconstruction in the presence of dopants, as well as both on the understanding of some fabrication steps of the nanovias, and on the dopants diffusion and characterization. Future work will also address the complete integration and assembly of a SOI and a silicon wafers,

and the measurement of the resistance of the whole electrical chain including nanovias and nanopads.

The presented achievements however already demonstrate the great potential of this technology and pave the way for the integration of nano-objects, from nano-electronics to bioelectronics.

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Designing Carbon Nanotube Interconnects for Radio Frequency Applications

Christophe Brun, Chin Chong Yap, Dominique Baillargeat and Beng Kang Tay

Abstract With the blooming demand for wireless and mobile applications, the needs to develop existing RF technologies are increasing. For example, there is a need for RF technologies that can operate at much higher frequencies, which can be potentially used for satellite or tetra-hertz imaging applications. Thus, there is a strong interest for novel materials, which can have more reliable and stable high-frequency performance. Flip chip is one of the technology offering lower insertion loss, compact packages, and low-cost fabrication. The use of carbon nanotube (CNT) bumps to replace existing materials or applications is not unheard of. In this chapter, demonstration of a successfully CNT flip chip device at high frequency will be done. A parametric study using hybrid EM/analytical modeling of the device will be conducted.

Christophe Brun and Chin Chong Yap contribute equally to this work.

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1 Introduction

Carbon nanotube (CNT) bumps had been demonstrated by several groups as potential off-chip interconnects [1–3]. Soga et al. [1] have shown the good mechanical flexibility and low bundle resistances of 2.3 Ω (for a 100-μm-diameter bump). Hermann et al. [3] have achieved reliable electrical flip chip interconnects using CNT bumps over 2000 temperature cycles. CNT bumps for practical applications such as high-power amplifier had also been demonstrated [2]. However, the use of CNT flip chip bumps tested for high-frequency performance is rarely seen. In this chapter, a novel unique joining process called CNT interconnection bump is demonstrated to achieve bonding between die and chip structures for pitch smaller than 150 μm, which is suitable for integrating RF components onto existing chips. Modeling and simulation will also be compared with experimental results to address the feasibility of CNT as transmission bumps for high-frequency applications. This is the first demonstration of a successfully CNT flip chip device at high frequency.

2 Common RF Measurements of CNT

For standard RF measurements, the transmission lines, and measurement tools such as the vector network analyzer, probes are all matched to 50 Ω. This poses a very serious problem to extract measurements and properties from 1-D material, such as CNT, which has already an inherent quantum resistance of 6.25 kΩ. The ratio of these two resistances is defined as a fine structure constant, α [4]. This fine structure constant is dependent on the charge of electron, the Planck's constant, and the speed of light. Because of this inherent mismatch, if the measurement is taken across a structure built with tapered coplanar lines filled with one or little CNTs across the signal structure, the reflection losses will usually be very high and the signal will be overcome by the background noise resulting in S_{21} below −15 dB [5].

Thus, special calibration techniques are needed to characterize CNT. The first approach is to use de-embedding technique [6], and the second approach is to design a structure with larger impedance [7]. The disadvantage of the latter approach is the amount of time and preparations required. Another method is to measure the change in high-frequency properties with a dc voltage, usually by fabrication transistors using the CNT [8]. The disadvantage of this approach is the accurate and reliability of the measurements.

Table 1 provides a summary of the various publication measurements of single-wall carbon nanotube (SWCNT), such as single, bundle, or very high density of SWCNTs as well as multi-wall carbon nanotubes (MWCNTs). Of these experiments, the most significant experiment was to fabricate a dense bundle of CNT to achieve 50-Ω-impedance matching. The large amount of work focusing on SWCNT was because of its ease of modeling and understanding of the fundamental

Table 1 Review on the experimental work for characterization of CNT found in literature

Refs.	Maximum measured frequency (GHz)	Type of CNT measured	Length of CNT (μm)	Findings
[9]	7	Single metallic SWCNT deposited using APTS on the gate electrode	1	Demonstrate high impedance (1 kΩ) characterization of CNT
[10]	40	Bundles of SWCNT by ac-dep	0.7	Model only valid up to 20 GHz. Calculated L_k is 7 % larger than theoretical and R_Q = 10.4 kΩ
[11]	20	Dense bundle of SWCNT by ac-dep	1	Achieved near 50 Ω impedance matching
[12]	20	Array of single SWCNT by CVD growth	2 and 9	Shown that the transmission power of CNT can be 30 dB higher
[13]	50	Array of SWCNT bundles by ac-dep	2	Extract the intrinsic properties of CNT using capacitive coupling
[5]	50	Single MWCNT by spin coating	5	MWCNT can transmit better ac signal at higher frequency
[6]	24	Single MWCNT transferred onto electrode followed by welding	7.5	Measured the impedance of MWCNT. Impedance decreases with frequency
[14]	67	Dense MWCNT array using ac-dep	2	CNT properties are independent of frequency up to 67 GHz
[15]	40	MWCNT bundles by CVD growth followed by planarization	10–30	Verified that L_k exists in the diffusive regime, scale with the length of CNT, and decrease with more CNT in parallel

properties. However, most of the reported work also focuses on short CNT (<10 μm). This is because the CNT solution used for ac-deposition is usually placed under sonication, resulting in the long CNT been cut into short length of less than 5 μm. On the other hand, it is a challenging issue to grow long bundles of CNT horizontally.

For the fabrication of CNT-FET, there are a bundle of papers in the literature; however, only a certain number is dedicated to extract high-frequency characteristics of CNT. Of these, the author found that one of the leading and more renowned groups is from Irvine and thus will mention more of their work in this section and shown in Table 2. One interesting modeling result for CNT is the ability to show that CNT can have high intrinsic speed limit and cutoff frequency at THz range [16].

Table 2 Review on experimental work for CNT-FET for RF properties

Refs.	Type of CNT measured	Findings
[8]	Single metallic SWCNT and single semi-conducting SWCNT	First demonstration of CNT operating at GHz frequency Perform measurement at room temperature and 4 K
[7]	Single semi-conducting SWCNT	Extracted Gm = 20 μS
[16]	Single SWCNT growth by CVD	Demonstrate CNT ability to carry high-frequency current as good as dc
[17]	Single CNT growth by CVD	Demonstration of CNT receiver
[18]	Single MWCNT	First successful operation of a MWCNT RF-set Develop a noise model

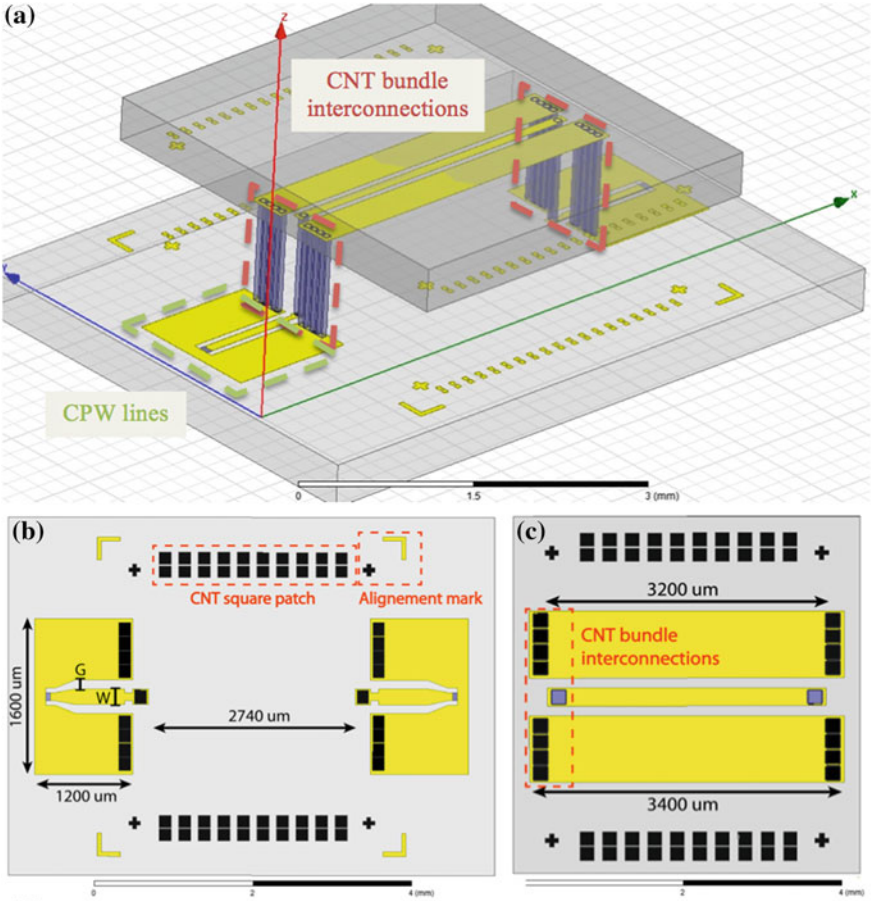
In this chapter, we will look at other approach using flip chip technology to characterize the RF properties of CNT bundles. The advantage of this method is the capability to measure long > 5 μm of CNT, and higher densities. The next section will discuss on the fabrication methodology and properties of the CNT flip chip test structures.

3 Design and Fabrication of Flip Chip Structure for High-Frequency Measurement

A flip chip structure composed of CNT bumps was designed to replace conventional metal bumps and characterized its performance up to 40 GHz as shown in Fig. 1a. When removed, the carrier comprises of "open" coplanar lines, while the chip is made of 50-Ω coplanar waveguide (CPW) structures. Three different sets of test structures were designed to demonstrate the feasibility of achieving fine pitch CNT bumps and their dimensions are given in Fig. 1d. The size of the signal line located at the chip was reduced to compensate for the parasitic capacitance between the two parts.

One thing to note in the design was that the CNT bumps for the signal and ground lines were deliberately designed to be rectangular shape, in order to compensate for the alignment accuracy of ±10 μm of the bonder machine. For example, the size of one bump on the carrier is 120 × 100 μm, while on the die is 100 × 120 μm. This enlarged bump area helped to decrease the occurrence of open circuitry and reduced the connection resistance due to misalignment [9]. The CNT bumps at the sides of both the carrier and chip act as dummy CNT bumps to enhance the mechanical strength of the CNT interconnection bump and hold the chip firmly. The number of CNT bumps/bundles on each design is also given. For smaller bump size, the number of bundles needs to increase accordingly [10].

The fabrication was then carried out using standard contact lithography and metal deposition systems. A schematic of the process is as presented in Fig. 2.



(d)

Structure	1 (170 μm by 150 μm)	2 (120 μm by 100 μm)	3 (70 μm by 50 μm)
W /μm	200	150	100
G /μm	115	87	61
Number of CNT bundle	58	74	94

Fig. 1 The schematic of the flip chip structure been fabricated to test both dc and RF functionalities. **a** The final flip chip after the chip is flipped and combined with the carrier, **b** carrier design which comprises of an "open" coplanar line structure, **c** chip design which comprises of coplanar line, **d** shows the variation of the size of 3 flip chip test structure

The starting substrate is a 4″ high resistivity (HR) <100> wafer with resistivity >10 kΩ. The use of HR wafer is necessary in RF application to minimize the attenuation loss [11]. Next, the wafers are cleaned and placed into the tube furnace

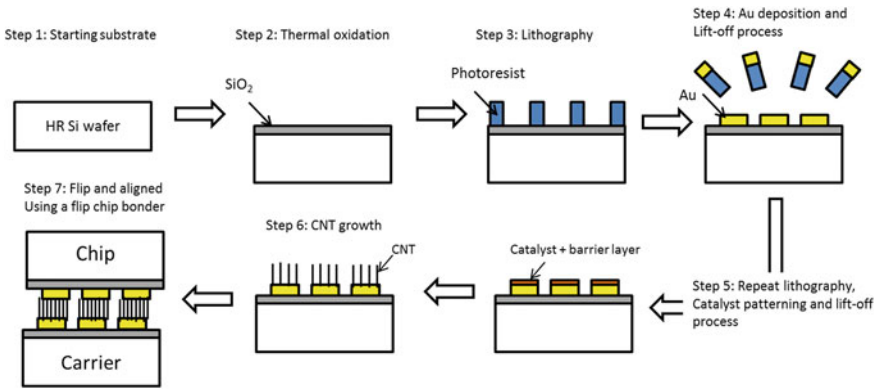


Fig. 2 The schematic of the flip chip structure fabrication process steps

to perform wet oxidation of 600 nm of SiO_2. The use of the SiO_2 layer is not necessary for RF application, but from a dc point of view, it is necessary to reduce the leakage current. Next, lithography patterning is performed to create the opening for the depositing of Au or Cu metallization by e-beam evaporation. After the first metallization is completed, a second lithography step is performed for the catalyst (used for CNT growth) and its barrier layer required for CNT growth [12–14]. The final 4″ wafer is then diced using a dicing machine and is ready for the growth of CNT. The CNT growths are then carried out in a PECVD system (Blackmagic PECVD system from Aixtron) at 650 °C. The final step is to use a flip chip bonder machine to align and assemble the final flip chip structure. The bonding load may be adjusted accordingly to achieve different penetration depth and dc resistance of the CNT bumps as depict in Fig. 3 [15]. Hence, the final flip chip device using interconnected bundles of CNTs has been achieved. A distance of 20-μm gap between the two parts was observed.

In order to extract the resistance of single CNT bump resistance, a four-point dc technique was used, with the concept shown in Fig. 4. The main advantage of using the four-point probe design is to eliminate the resistances of the probe pins and metal lines, thus removing unwanted resistances from the CNT bump measurements. The resistance of the metallization was found to be in the same order as the

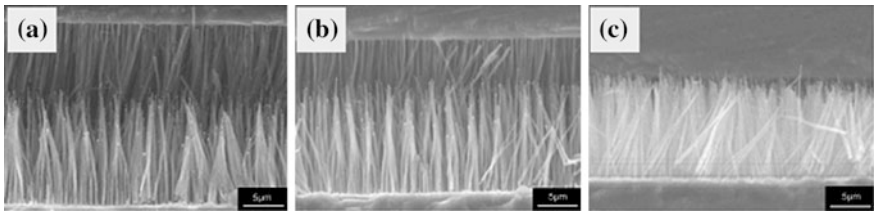


Fig. 3 Interconnection length regarding the force applied: no load (**a**), 0.03 g (**b**) and 3 kg (**c**). At 3 kg, the interconnection length is at maximum

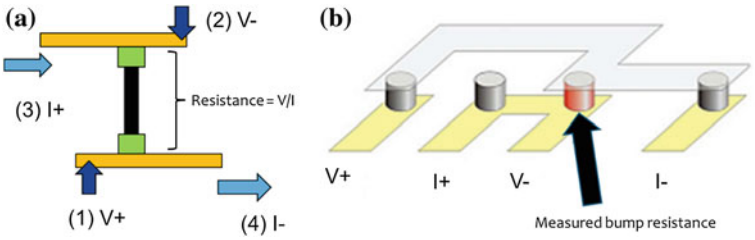


Fig. 4 The concept of four-point probe measurement techniques

CNT bump resistance in our experiments; this is an important step that must not be neglected. By sending a current to the pad at point 3 and 4, the voltage across the point of interest can be measured as shown in Fig. 4a. One important assumption in these measurements is that there is current that flow through (1) and (3) due to the infinite internal resistance of the voltmeter. The resistance of the bump can then be calculated by dividing the measured voltage over the input current. More information on the dc measurements can be found in other publications' records [3].

To further improve the electrical performance of the CNT interconnection bumps on metal, the choice of barrier layer is very crucial. Using Ti and TiN as the barrier layer in our study, Ti/TiN was found to be a better choice as compared to using TiN barrier layer. This is due to better conductivity of Ti and Ti is a preferred choice of adhesive layer for various metals in the industries. In Fig. 5b, it was also observed that the resistance decreases when the barrier layer thickness decreases. It further shows that electrons tunnel through the barrier layer and affect CNT conductivity. By comparing the resistivity values, the resistivity extracted was 0.164 Ω cm for the 30 s Ti/30 s TiN, 5.175 Ω cm for the 3 min Ti/60 s TiN, and 0.695 Ω cm for 5 min TiN barrier layer. This clearly shows that thinner barrier layers help to improve the CNT conductivity.

High-frequency measurements from 1 to 40 GHz are also performed on the flip chip structures. Measurements are run with a vector network analyzer (VNA) Agilent HP8510C and 150-μm-pitch Cascade Microtech Infinity probes.

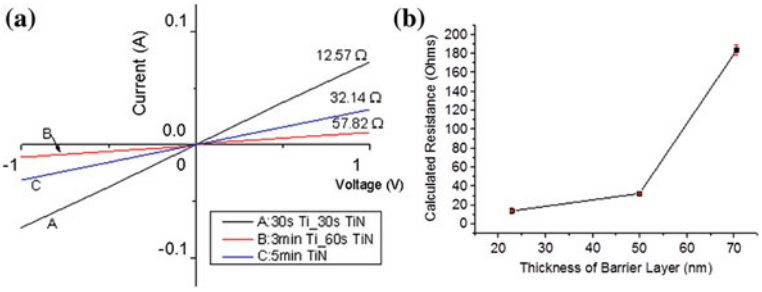


Fig. 5 **a** The resistance of CNT bump on 3 different barrier layers. The results on 30 s Ti/30 s TiN give the lowest resistance. **b** Variation of the CNT bump resistance with thickness of barrier layers

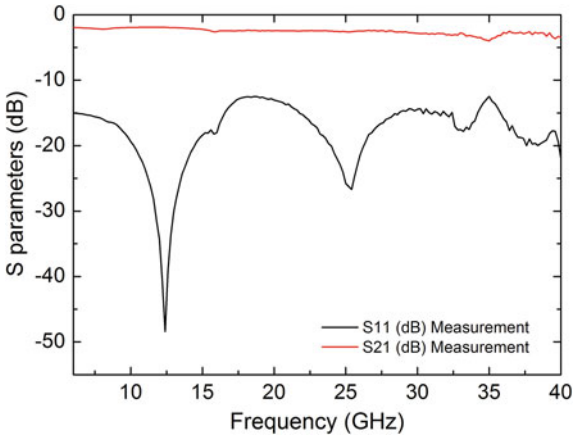


Fig. 6 *S*-parameter measurements (*solid lines*) of the flip chip device between carrier input and output. Maximum return loss of −13.5 dB is reached at 18 GHz

A thru-reflect-line (TRL) calibration process is done before each measurement with a maximum error bar equal to 0.1 dB. TRL is a calibration process done before a high-frequency measurement by a VNA. This calibration process consists of replacing the device under test by a thru line, a short circuit, and finally a load circuit at 50 Ω. After this calibration, the losses caused by the equipments (cables, probes, …) will be omitted.

As shown in Fig. 6, flip chip device exhibits S_{21} parameters of −1.21 and −3.69 dB from input to output of the flip chip structure operated from 1 to 40 GHz. For the first time, this later gives the proof of high-frequency transmission in the flip chip device composed by CNT bundles. The return loss (S_{11}) stayed below −13 dB. The small variations above 30 GHz are due to the calibration process, which returns a measurement error between 0.1 and 0.2 dB at some frequency points.

4 Flip Chip Modeling by Electromagnetic/Analytical Approach

The flip chip structure is studied using a hybrid approach based on the 3-D electromagnetic (EM)/circuit modeling between 1 and 40 GHz. The hybrid approach combines advantages from both EM and circuit/analytical models, giving more accuracy, and allows better control of the model parameters such as the analytical model of the CNT bundles. In this modeling work, several CNT parameters such as CNT diameter, length, bundle density, and other CNT components can be easily tuned. More details will be described later. An optimization of the flip chip performance becomes possible as well and will be presented on the second part.

4.1 Modeling of Flip Chip Device

4.1.1 EM Modeling of the Flip Chip Device Without the Interconnections

To conduct the hybrid EM/analytical simulation of the flip chip device, all the structures, except the CNT bumps, are first considered by 3-D EM simulations to define a generalized matrix [SG]. [SG] is defined between input/output 50-Ω-lumped ports (port 1 and port 2) and internal 100-Ω-lumped accesses (3–6) for connecting circuit models of CNT bumps (Figs. 7 and 8). EM simulations are performed by software Ansoft HFSS based on the finite element method. In Fig. 7, printed circuit board is visible on the left and die part is shown in right. Black pads represent the CNT bundle locations. Red pads correspond to the lumped ports for EM simulations and *S*-parameters matrix extraction. In Fig. 8, [SG] represents the matrix extracted from the EM simulation of the flip chip structure. "RLC transmission line" boxes correspond to the CNT bundle model that will be presented on the next paragraph. $R_{CNT\text{-}CNT}$ is the contact resistance between the interconnected CNTs. We will use the value of $R_{CNT\text{-}CNT}$ = 324 kΩ, extracted from the previous study of the flip chip device [16].

4.1.2 Analytical Modeling of the Two Interconnected Bundles of CNTs

The circuit model based on a RLC transmission line describing the electrical behavior of the CNT structure is presented in Fig. 8. Also visible on Fig. 8, the CNT circuit models are inserted between the lumped accesses (ports 3–4 and ports 5–6) of the flip chip matrix [SG]. The RLC transmission line is composed by lumped and distributed components as described in this Ref. [17]. The contact

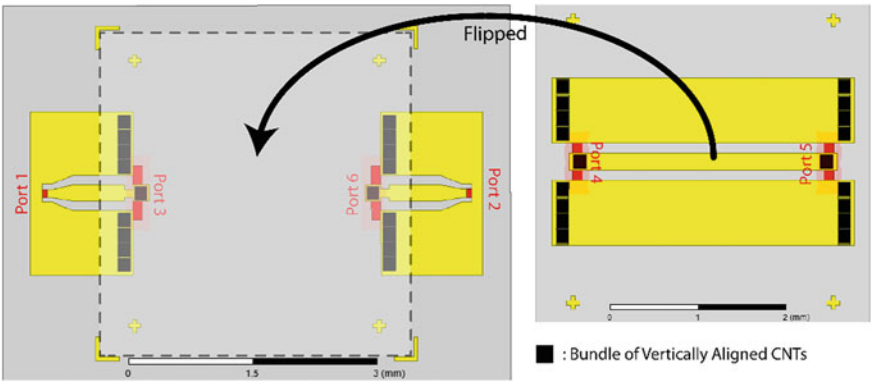


Fig. 7 Top view of the schematic of the flip chip structure

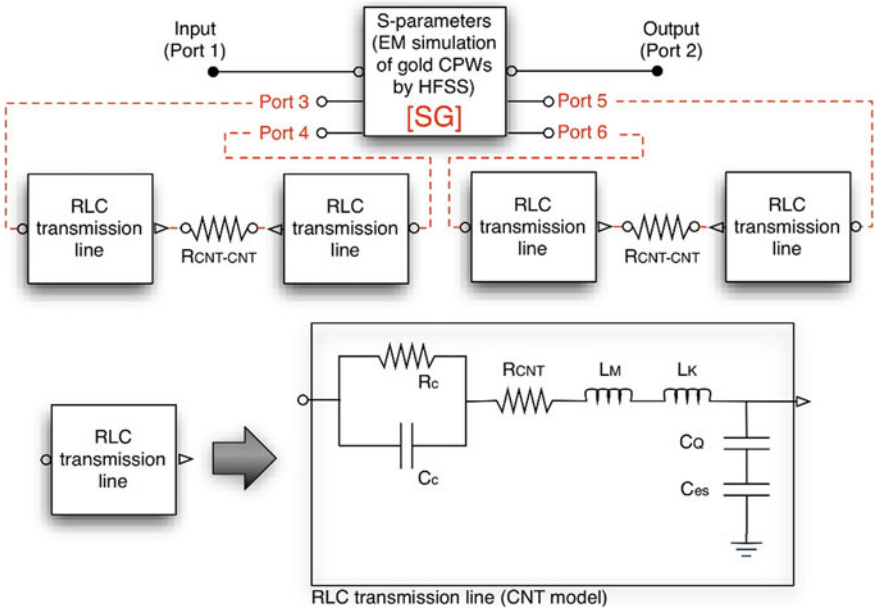


Fig. 8 Diagram of the hybrid flip chip structure model

capacitance C_C and the contact resistance R_C model the contact between the CNTs, and the metal and values are found according to the other works [18].

All component values are visible in Table 3. A quantum-distributed resistance derived from $R_{\text{CNT-bundle}} = \frac{h}{2e^2} \times \frac{1}{N_{\text{channels/MWCNT}} \times N_{\text{CNT}}} \times \frac{l}{\text{MFP}}$ represents losses along the CNT (h: Planck's constant; e: elementary charge; l: CNT length; and MFP the mean free path). However, in our model as presented in Fig. 8, a quantum resistance of R_{CNT} = 20 kΩ/μm is used because of the experimental work [19] showing a higher resistance in CNTs than the one predicted. This higher resistance than the one predicted is mainly due to the higher level of impurities in CNTs fabricated by PECVD process. The two other distributed components for nanowire effects are added: a kinetic inductance $L_k = L_{\text{k-bundle}} = \frac{h}{2v_F} \times l \times \frac{1}{N_{\text{channels/MWCNT}} \times N_{\text{CNT}}}$ and a quantum capacitance $C_Q = C_{\text{Q-bundle}} = \frac{2e^2}{hv_F} \times l \times N_{\text{channels/MWCNT}} \times N_C$ ($v_F = 9.7 \times 10^5$ m/s: Fermi's velocity).

In CNTs, the electron transport is quantized on a finite number of conducting channels. Consequently, there are a finite number of conducting channels in CNTs

Table 3 CNT bundle component values

N_{MWCNT}	R_C	C_C	R_{CNT}	L_K	$R_{\text{CNT-CNT}}$
1	10 kΩ	4.1×10^{-6} aF	20 kΩ/μm	0.86 nH	324 kΩ
1.35×10^5	74 mΩ	55 pF	0.15 kΩ/μm	6.34 fH	2.4 Ω

regarding the dimensions (radius, number of shell). In order to calculate the number of conducting channel $N_{\text{channels/MWCNTs}}$ in the 100-nm-diameter MWCNTs, we start to calculate the diameter of a specific shell in a MWCNT, by using the Eq. (1) [20]:

$$D_i = D_{\max} - 2d(i-1) \quad \text{with} \quad 1 \le i \le p \tag{1}$$

where i is the shell number and d is the gap distance between shells also called VDW distance. $i = 1$ will correspond to the outer shell, while $i = p$ will be the inner shell in the MWCNT. Finally, in order to estimate the number of conducting channel in a specific shell, we use the Eq. (2) [20, 21]:

$$N_{i\text{-channel/shell}} = aD_i + b \quad \text{with} \quad D > 3\,\text{nm} \tag{2}$$

where a = 0.0612 nm^{-1}, D_i: MWCNT-selected shell diameter, and b = 0.425. Finally, we have to sum up all the channels existing in the MWCNT, and we will obtain $N_{\text{channels/MWCNT}}$:

$$N_{\text{channels/MWCNT}} = \sum_{i=1}^{p} N_{i\text{-channels/shell}} \tag{3}$$

Thus, after calculation, there are 74 shells and $N_{\text{channels/MWCNT}}$ = 374 conducting channels in a 100-nm-diameter MWCNT.

The magnetic inductance L_{M} is considered negligible compared to the very high kinetic inductance L_{k} in nanowires [17]. Electrostatic capacitance C_{ES} represents the coupling effect between the ground plane and the CNT. Both C_{ES} and C_{Q} are calculated with the number of CNTs in the outer bundle layer [N_{C}, Eq. (4)]. We can estimate the number of circumferential CNTs N_{C} = 3000 located at the edge of the square bundle by the Eq. (4):

$$N_{\text{C-square}} = \frac{4(c - d_{\text{CNT}})}{d_{\text{CNT}}} \tag{4}$$

where c is the side dimension of the square bundle and d_{CNT} is the CNT diameter. Because N_{C} = 3000 is low and the distance between the signal bump and the ground bump (163 μm) is important compared to the MWCNT diameter (100 nm), C_{ES} and C_{Q} can be neglected. In order to model a bundle of CNTs, we also consider the coupling between CNTs weak because of the large distance between them (about 200–500 nm). Then, the RLC CNT models are placed in parallels according to the estimated number of CNTs $N_{\text{MWCNT}} = 1.35 \times 10^5$ in the bundle as defined in the previous part.

As shown in Fig. 9, a good agreement is found between simulations and measurements. With the hybrid model, we have directly access to all CNT components such as the contact resistance and capacitance, the CNT resistances, and inductance. As we will see in the next part, this hybrid model is easily tunable and allows us to exploit different configuration of CNT bundle. The number of CNT placed in

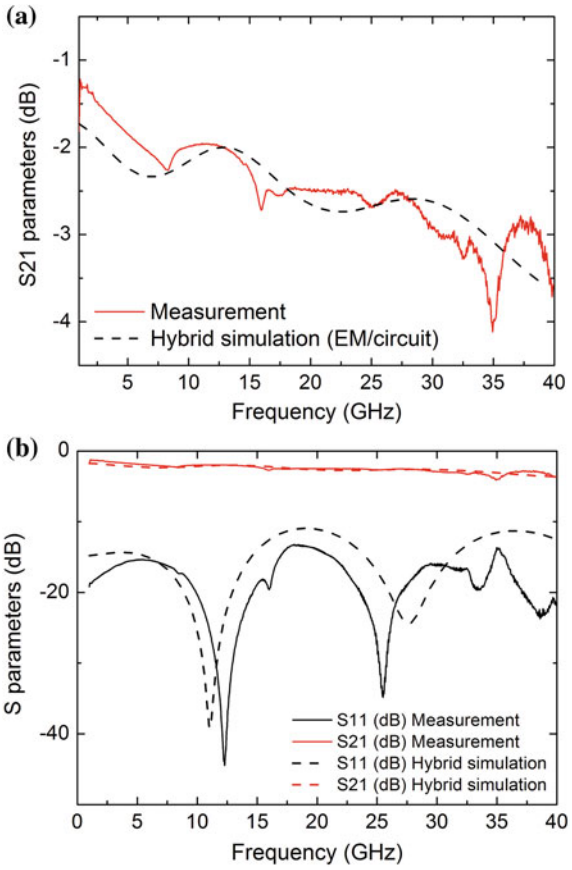


Fig. 9 *S*-parameters of the flip chip structure measured between port 1 and port 2. *Solid lines* correspond to the measurements, while dash lines show the hybrid EM/circuit simulation results

parallel in the bundle can compensate for this high contact resistance. The measured CNT bundle resistance is found at 6.25 Ω with 135,000 estimated interconnected CNTs.

4.2 Parametric Study of the Flip Chip Using the Hybrid EM/Analytical Model

In this part, we will proceed to a parametric study of our flip chip structure using the analytical MWCNT bundle model we presented earlier. To proceed, we keep our EM simulation of the flip chip structure without the bumps. Figure 11 shows the results of this EM simulation where the ports (3 and 4) are directly linked to ports

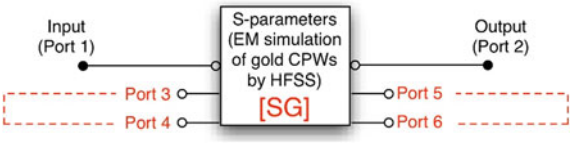


Fig. 10 Schematic of the full-EM flip chip simulation without bumps

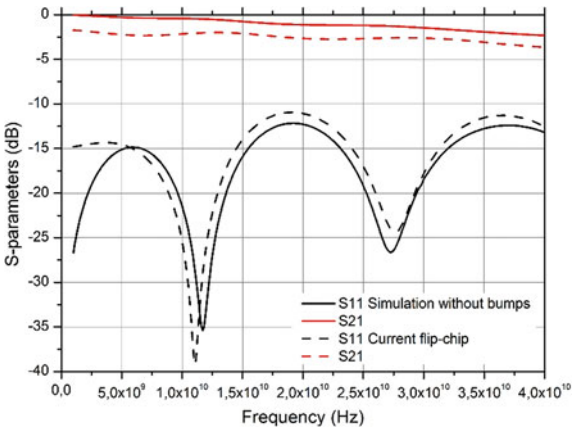


Fig. 11 *S*-parameters of the full-EM simulation of the flip chip structure without bumps according to the schematic in Fig. 10

(5 and 6) and ports (7 and 8) are directly linked to ports (9 and 10) according to the schematic visible in Fig. 10. Again, ports 1 and 2, respectively, represent the input and the output of the flip chip device. Thus, the best results we can expect to obtain with insertion loss S_{21} and return loss S_{11} for our flip chip structure are those presented in Fig. 11. As illustrated, insertion losses S_{21} from −0.045 to −2.3 dB has been obtained from 1 to 40 GHz. It is interesting to highlight that these results are consistent with the measurements of the CPW lines alone done previously. Indeed, losses from −1 to −2 dB had been achieved. We show that the measured resistance of 12.5 Ω is mainly due to the CNT bundles.

Different CNT bundle parameters will be tuned in order to execute our parametric studies. Since we have shown that our CNT bump acts mostly like a resistance, we will focus on these components. First, we will modify the contact resistance between CNT $R_{\text{CNT-CNT}}$; secondly, we will change the distributed CNT resistance R_{CNT}; and finally, we will tune the CNT density. The CNT length cannot be modified since another full-EM simulation of the flip chip structure must be performed for each new distance between the two parts according to the new CNT length.

4.2.1 Parametric Study on the CNT Resistance R_{CNT}

In this first parametric study, the value of the CNT resistance R_{CNT} is modified. With the flip chip presented previously, we had $R_{CNT} = 20$ kΩ/µm, and as explained previously, this value is quite high as compared to the theoretical values. We decided to try two values of CNT resistance: 0 and 10 kΩ/µm. We can imagine reaching 10 kΩ/µm by improving our CNT fabrication process and hence decrease the number of impurities in our CNTs. With 0 kΩ/µm, we reach the theoretical resistance value of a perfectly structured MWCNT. A MWCNT without impurities can have a mean free path up to 20–25 µm [22], which is approximately the length of our MWCNTs in our flip chip device. Thus, if we are below the MFP length of the MWCNT, no scattering will occur during the electron propagation, and electrons follow a ballistic transport along the CNT. So, the 0 kΩ/µm represents the ideal case we could expect to achieve with a perfect control of the CNT fabrication process.

As seen in Fig. 12, the insertion loss S_{21} does not improve significantly even though the CNT resistance (black dash curve) has been halved. Thus, only an increase of 0.5 dB is visible in low frequency (1 GHz) and an increase of 0.25 dB at high frequency (40 GHz). Moreover, as observed in Fig. 12 represented by the blue dash curve, even with no CNT resistance, the S_{21} increased by 1 dB at 1 GHz and by 0.5 dB at 40 GHz.

In conclusion, by improving our CNT fabrication process and so decrease the CNT resistance, we show that we are able to improve the performance of our flip chip. However, we can also observe that the CNT resistance is not the main factor affecting the loss of our device. We will see on the two next sections how the other components also affect the RF performance.

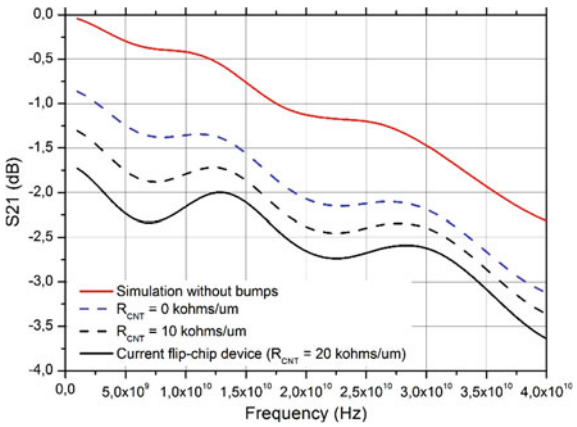


Fig. 12 S_{21} parameter of the hybrid EM/analytical flip chip simulation with a parametric study on the CNT resistance R_{CNT}

4.2.2 Parametric Study on the CNT Contact Resistance $R_{CNT\text{-}CNT}$

In this second parametric study, we modify the contact resistance between CNT $R_{CNT\text{-}CNT}$ from its current value of 324–0 kΩ. As observed from Fig. 13, showing the insertion loss of the flip chip with the different values of $R_{CNT\text{-}CNT}$, by dividing by 3 times $R_{CNT\text{-}CNT}$ (black dash curve), we only improved the S_{21} by 0.5 dB at low frequency (1 GHz) and by 0.25 dB at higher frequency (40 GHz). With $R_{CNT\text{-}CNT}$ = 1 kΩ, we improve again S_{21} by 0.25 dB on all the bandwidth (purple dash curve). Thus, we observed that by decreasing the contact resistance between CNTs alone is not sufficient for improving more than 0.5 dB the S_{21} transmission.

Finally, we decided to model a case where we have neither any contact resistance between CNTs nor distributed CNT resistance, which should be possible with perfectly structured MWCNTs without impurities and a MFP near 25 μm as we explained in the previous part. In this case, in Fig. 13 (blue dash curve), we almost reached the level of performance of the flip chip without CNT bumps. Indeed, the S_{21} insertion loss was increased by 1.25 dB at low frequency (1 GHz) and by 1 dB at higher frequency (40 GHz).

In conclusion, an important work needs to be done on the CNT qualities by improving the fabrication process. An increase of the process temperature would increase the catalyst clusters temperature and consequently decrease the number of impurities in CNTs [23]. Then, instead of decreasing the contact resistance between CNTs, we can imagine to increase the number of contact and hence achieve a level of performance near the red curve in Fig. 13. By working on the both aspects (fabrication process and CNT contact density), we can imagine to reach a very good level of performance for our flip chip based on the CNT interconnections with an S_{21} parameter from −0.5 dB at 1 GHz to −2.5 dB at 40 GHz.

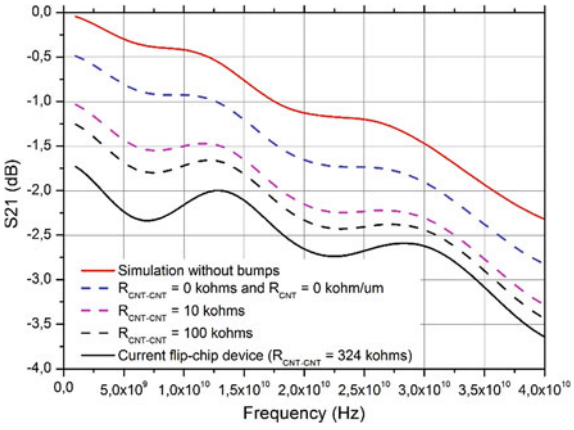


Fig. 13 S_{21} parameter of the hybrid EM/analytical flip chip simulation with a parametric study on the CNT contact resistance $R_{CNT\text{-}CNT}$

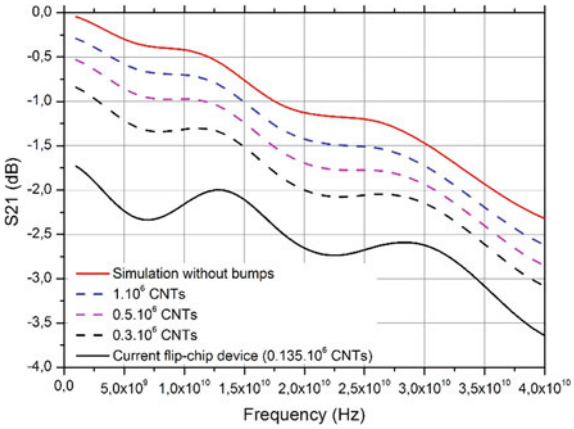


Fig. 14 S_{21} parameter of the hybrid EM/analytical flip chip simulation with a parametric study on the CNT density

4.2.3 Parametric Study on the CNT Density (N_{MWCNT})

Finally, we modify the CNT density (N_{MWCNT}) in the bundle from 0.3×10^6 to 1×10^6 CNTs. As observed from Fig. 14, by having twice the CNT density (black dash curve), we already improve our S_{21} parameter by 1 dB at 1 GHz and 0.5 dB at 40 GHz. Indeed, as we already explained and observed in the two previous parts, we need to improve the contact resistance between CNTs in the same time than the CNT resistance. Thus, by increasing the CNT density, we are working on the two parameters on the same time: We decrease the total resistance by increasing the number of contact and we decrease the total CNT resistance by decreasing the number of CNTs in the bundle.

And the two other curves confirm this observation (purple and blue dash curves) and show an important increase in the S_{21} parameter with the increase in the CNT density. With a CNT density of 1×10^6 CNTs (blue dash curve), we achieve insertion loss from 0.25 dB at 1 GHz to −2.5 dB at 40 GHz, which is very close to the optimal results we could obtain visible on the red curve.

In conclusion, focusing on the CNT density might be the best choice to improve the performance of our flip chip. We can improve the CNT density by modifying the catalyst layer thickness with PECVD process. Thus, with a number of 1×10^6 CNTs or above, which represents a density of 44 CNT/μm^2, we could reach higher flip chip performance using CNT interconnections.

5 Discussion and Future Works

In conclusion of this study, several techniques to characterize CNTs as interconnections have been presented. The use of packed bundle of CNTs appeared to be the best option to override the high intrinsic CNT quantum resistance. However, to

make this option viable, a uniform bundle of CNTs in terms of length, diameter, and CNT quality must be achieved in order to be able to extract later the CNT parameters. Thus, a CVD/PECVD approach has been chosen to grow vertically aligned bundle of MWCNTs. CVD/PECVD processes return the best characteristic to achieve uniform bundle of CNTs with a good control of the CNT orientations and parameters such as the diameter and length.

A flip chip device has hence been designed based on the PECVD growth of square bundles of vertically aligned MWCNTs on RF metallic structures. The flip chip proposed an innovative way to interconnect a die on a carrier by using a combination of the electrostatic and Van der Waals forces to attach the grown CNTs to each other. Thus, an electric bond was created without the use of any heating or paste substances. dc and RF characterizations up to 40 GHz have been conducted in order to verify the feasibility of the flip chip device based on the interconnected bundles of CNTs. The performances of this innovative flip chip are encouraging but still lower than the degree of performance that can be obtained with metal bumps at these frequencies.

Finally, a hybrid EM/analytical model has been developed to fit the RF measurements of the flip chip device. Component values based on the CNT transmission line circuit model were extracted from theoretical studies and literatures. The quantum resistance of the fabricated CNTs appeared to be higher than the one expected in theory. Thus, future work must first focus on the quality of the fabricated CNTs by PECVD in order to improve the performance of the devices dedicated to RF. Moreover, additional studies on the flip chip performance using the tunability of the components composing the hybrid model have demonstrated that not only the CNT resistance needs to be reduced, but also the number of interconnected CNTs must be increased. Thus, several points need to be improved at the same time in order to reach performance of the flip chip based on the metal bumps. In the near future, by optimizing all aspects of the CNT growth by PECVD (bundle density, CNT quality, and uniformity), CNTs will become a serious competitor for making interconnections dedicated to RF devices.

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Packaging of Buckyballs/Buckytubes in Transparent Photo-Active Inorganic Polymers: New Hope in the Area of Electronics and Optoelectronics

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Abstract Pb-phosphate glass-based optically transparent and light sensitive two composites, one containing C_{60}-fullerene and the other single-walled carbon nanotubes (SWCNTs), have been prepared by melt-quenched technique, and their optical, electronic, and optoelectronic properties have been studied. Absorption studies of the SWCNT-composite show that the SWCNTs in this system suffer massive conformational deformations and as consequence band structure modulations. Conductivity measurements have revealed that the presence of SWCNTs in the host glass, which is basically an insulator, increases the conductivity of the host almost by hundred thousand times. UV–Vis light-induced absorption (LIA) and UV–Vis light-induced ESR (LIESR) studies in the case of C_{60}-composite and similar LIESR and conductivity studies in the case of SWCNT-composite show that both the composites suffer a light-induced charge separation phenomenon, which involves electron transfer from the divalent (Pb^{2+})-center of the host to their respective electron acceptor (C_{60}/SWCNT). Related charge transfer products are: Pb^{3+}-holes and C_{60}-anions in the case of the fullerene composite; and Pb^{3+}-holes and conduction electron rich SWCNT anions in the case of the SWCNT-composite. The conductivity properties of the SWCNT-composite, suggest a possibility of its use as a transparent electrode, while the photo-induced charge—separation phenomenon of both the composites indicates prospect of their use as solar photo → current converter.

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1 Introduction

Transparent conducting coatings are essential components of many electro-optical devices. Considering the good electron-conduction properties of SWCNTs, researchers were interested to develop SWCNT-based transparent conducting coatings [1, 2] since the discovery of the methods of its successful synthesis [3]. Metallic SWCNTs are almost six times more conducting than that of its semiconducting counterpart [2]. So it is desirable that the developed transparent conducting coatings be rich in metallic SWCNTs. Unfortunately, an as synthesized sample of SWCNTs, always contains both its semiconducting and metallic varieties which are difficult to separate. Various approaches [4–6] to modulate the band structure of SWCNTs from semiconducting to metallic have been proposed. One of these approaches is the stress-induced band structure modulation through structural deformations. Strains such as compression, uniaxial stretching, and torsion on SWCNTs may bring about a change in their band structures from semiconducting to metallic. In the first section, we will discuss about one of our recent studies on the development of an optically transparent quasimetallic SWCNT/inorganic glass composite for possible use as transparent electrode. We used in this case, the internal tress of the inorganic host to modulate the band structure of a commercial sample of SWCNTs almost completely to a quasimetallic type by incorporating the latter in to the matrix of the former.

SWCNTs and fullerenes are also known to be good electron acceptor in the presence of a suitable donor [7–9]. Such property of both SWCNTs and fullerenes is useful for generating photo-induced charge separation by incorporating them in a suitable photo-generating medium such as organic conjugated polymers. Photo-induced charge separation being the fundamental process of all photovoltaic (PV) cells, there have been several studies on the development of organic conducting polymer/fullerene or conducting polymer/SWCNT photovoltaic cells [7–9]. Organic polymers are chemically unstable and prone to photo-degradation [10], and their light absorption efficiency (η_A) in the visible region is also low. So a practically useful fullerene or SWCNT containing conducting polymer-based PV-device is yet to come up. Search for a new type of photo-generator other than organic polymers thus seems to be essential. Photo-active inorganic polymers such as inorganic glasses may be one of the possible alternatives. It is well known that in the case of a high Pb-containing phosphate or silicate glass, a large fraction of the lead remains as Pb^{2+} ions in the interstices of the glass structure. These interstitial Pb^{2+} ions are very sensitive to radiations ranging from γ-ray to UV–Vis light [11, 12] and generate Pb^{3+} holes and free electrons in the matrix by the action of the incident photons. These irradiation-generated electrons, in a normal case, are captured by the network Pb^{2+} ions [(P–O–Pb–O–P)/(Si–O–Pb–O–Si)] of the glass itself and create trap centers of the type $(P–O–Pb–O–P)^{-}$/$(Si–O–Pb–O–Si)^{-}$ [13]. However, in the presence of an added strong electron scavenger in the glass, the irradiation-generated electrons are captured mainly by the added scavenger [12, 14] and the formation of $(P–O–Pb–O–P)^{-}$ like trap centers in the matrix is inhibited.

So, a Pb-based inorganic glass may be considered as an alternative to the photo-generating organic polymers. Here, we also discuss about our recent studies on the generation of UV–Vis light-induced charge separation in two Pb-phosphate glass-based composites one containing fullerene and the other SWCNTs.

2 Experimental

2.1 Material's Synthesis

C_{60}-fullerene/glass composite was prepared by melting a mixture of frits of a previously prepared (Pb, Zn)-phosphate glass and C_{60}-fullerene (Lancaster, UK) in an atmosphere-controlled furnace at a temperature of 750–800 °C and subsequently quenching the melt under controlled atmosphere. Fullerene concentration in the composite was found to be 5.10^{-5} M.

SWCNT–glass composite was prepared in a similar way by using a mixture of carboxylic acid-functionalized SWCNT bundles (Sigma Aldrich; individual nanotube's diameter range = 1.3–1.5 nm and length 0.5–1.5 μm) as a precursor of SWCNT and the frits of a similar (Pb, Zn)-phosphate glass. To eliminate the carboxylic acid groups from the precursor carboxylic acid-functionalized SWCNTs by thermal decomposition and simultaneously to keep the resulting hydrogenated SWCNTs encased in the glass matrix, the mixture was first heated at 350–400 °C (above the T_g = 315 °C of the glass) for several hours under suction until a sintered composite mass was obtained. The temperature was then raised to 760−770 °C to melt the sintered composite to a fluid as well as to convert the hydrogenated SWCNTs into pristine SWCNTs by removing the hydrogen. The melt was then rapidly quenched to a monolithic transparent solid. Details of the method are described in [5]. The concentration of SWCNTs in the composite (density = 4.33 g cm^{-3}) was calculated to be 2.54×10^{-4} g% (W).

To make a comparative study of the optical and electronic properties of the SWCNTs of the composite with those of the pristine SWCNTs, a film of SWCNTs was also prepared by using a solution of the same carboxylic acid-functionalized SWCNTs. The film was deposited on a borosilicate glass slide by the stain drawing method. The carboxylic acid groups of the SWCNTs of the film were subsequently thermally decomposed by heat treatment at 400 °C in an inert atmosphere for 2 h, and the resulting hydrogenated SWCNTs were then converted to pristine SWCNTs by removing the hydrogen at 600 °C.

2.2 Methods

The high-resolution transmission electron micrographs (HRTEM) of the composite samples were recorded in a 300 kV HRTEM (model: JEM-2011, make: JEOL, Japan). The thickness of the SWCNT-film was measured by an atomic force

microscope (AFM). All absorption spectra were recorded at 300 K in a UV–Vis–NIR absorption spectrophotometer (Shimadzu, Model 3001). In the case of light-induced absorption (LIA) study of the fullerene composite, a rectangular-shaped polished sample (25 mm × 15 mm × 3 mm) was first irradiated with UV–Vis (230–400 nm) light from a 125-watt Hg lamp (Hanovia, USA) for 90 min, keeping the sample at a distance of 15.0 cm from the source. A UV transmitting (230–400 nm) filter (Oriel, USA) was used to cut off the visible part of the source. The LIA spectra of the irradiated sample were then measured at 300 K as a function of time.

ESR spectra of the composites were recorded at 300 K in an X-band electron spin resonance spectrometer (model: JEOL JES-FA200, Japan). In the case of fullerene composite, the sample was first irradiated with UV–Vis (230–400 nm) light from the same 125-watt Hg lamp, and then, its ESR spectrum was recorded at 300 K.

In the case of the SWCNT-composite, the ESR spectra were recorded in the presence and in the absence of UV–Vis illumination. A 150-W xenon lamp was used to illuminate the sample. The lamp was placed at a distance of approximately 28 cm from the sample cavity.

All electrical measurements with and without UV–Vis illumination of the composite were carried out using a picoammeter (model: 6487, make: Keithley, USA) provided with a voltage source. The same Xe lamp mentioned above was used to illuminate the sample during its light-induced electronic property studies.

3 Results and Discussions

3.1 SWCNT/Inorganic Glass Composite: Stress-Induced Metallization of SWCNTs in the Host and Its Application as Transparent Electrode

A HRTEM of the SWCNT/glass composite synthesized by incorporating SWCNTs into the matrix of a (Pb, Zn)-phosphate glass is shown in Fig. 1.

The presence of randomly oriented both isolated and bundles of SWCNTs in the matrix is clearly visible. A simple calculation [5] based on the diameter distribution data (1.3–1.5 nm) of the SWCNT sample used indicated that the SWCNTs present in the composite were of (10, 10), (11, 11) armchair metallic, (18, 0) zigzag quasimetallic, (17, 0), (19, 0) zigzag semiconducting, and other semiconducting nanotubes of different chiralities.

The base glass corrected absorption spectrum of SWCNTs in the composite is shown in Fig. 2, along with that of the host glass. The absorption spectrum of the SWCNT-film prepared by using a solution of the same sample of SWCNTs is also shown in the figure. A picture of a polished transparent sample of the composite is shown in the inset. The spectrum of the SWCNT-film exhibits two broad absorption

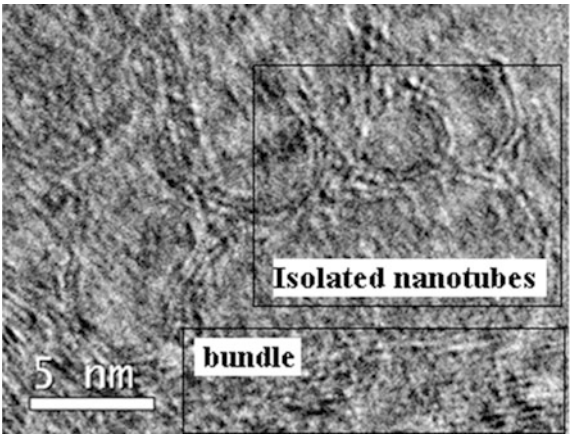

Fig. 1 HRTEM of a sample of the SWCNT/glass composite (after Ref. [5])

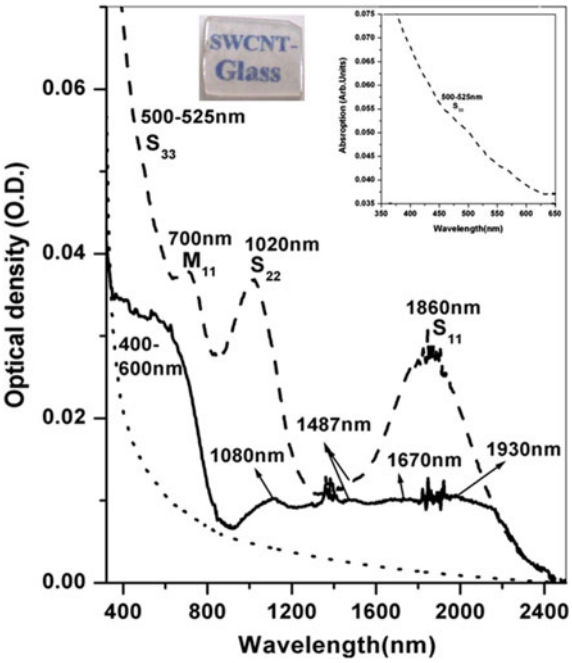

Fig. 2 (*Solid line*), base glass corrected absorption spectrum of SWCNTs of the composite; (*Dotted line*), that of the base glass at 300 K (sample thickness in each case $\sim 0.09 \pm 0.01$ cm); (*Dashed line*), absorption spectrum of the SWCNT-film (d $\sim$ 2.1×10^{-5} cm). *Inset*: *left*, a photograph of a polished sample of the composite; *right*, a more resolved 500–525 nm absorption shoulder of the SWCNT-film (after Ref. [5])

bands peaking, respectively, at around 1860 nm (0.66 eV) and 1020 nm (1.2 eV), and a relatively narrow band with maximum at ~700 nm (1.77 eV). The spectrum also shows a high-energy absorption shoulder at ~500–525 nm (2.48–2.36 eV) on the tail of the strong π-plasmon absorption of the nanotubes.

The absorption bands observed in the spectrum of the film are actually the average absorption characteristics of different types of SWCNTs present in the film. The two low-energy bands and the high-energy absorption shoulder may be assigned [15] as the transitions across the band gaps of the first, second, and third pairs of one-dimensional van Hove singularities of the density of states of different semiconducting SWCNTs, which are marked as S_{11}, S_{22}, and S_{33}, respectively. The band observed at ~700 nm (1.77 eV) is actually identified [15] as the first-order metallic/quasimetallic transitions of the SWCNTs. It is evident from the spectrum of the glass component of the composite that the host glass itself has no distinct absorption band in the 400–2400-nm wavelength region. So the absorption bands those are observed in the spectrum of the composite are the absorption characteristics of its SWCNTs only. Comparing the spectrum of the composite with that of the SWCNT-film, it can be noted that the absorption bands of the SWCNTs of the composite suffer a drastic change in respect of both energies and relative intensities. The S_{11} semiconducting band suffers a broadening concomitant with a lowering of intensity. Within this broad band, a number of poorly resolved weak bands at 0.64 eV (~1930 nm) and 0.74 eV (~1670 nm), distributed over lower and higher energy side of the 0.66 eV (1860 nm) S_{11} band of the SWCNTs of the film, are noted. Similar broadening and lowering of intensity in the case of the S_{22} band are also observed. A change in the case of semiconducting S_{33} absorption is also noted. It is found to lose its intensity and mingle with the M_{11} metallic band, which also shifts to higher energy without making any significant loss in its relative intensity. The S_{33} band and the shifted metallic band on mingling together create a broad absorption feature in the 400–600-nm spectral regions. Thus, it is evident that the band-gap energies of the semiconducting nanotubes of the composite have suffered both increase and decrease in their values, while the first-order metallic bands of its metallic nanotubes show a phenomenon of opening a gap at their Fermi energy. Considering the fact that the composite was synthesized by rapid quenching a melt of a mixture of the glass and the SWCNTs from 1033–1043 to 300 K, generation of various types of stresses inside the composite is quite possible. The observed drastic changes in the band structure of the SWCNTs of the composite, therefore, most likely seem to occur due to their structural deformations by the internal stress of the host which is generated during the quenching of the composite melt. Phenomenon of stress-induced deformation and consequent modulation of band structure of SWCNTs has been predicted theoretically and subsequently proved by experiments by many earlier workers [4, 5]. The linear thermal expansion coefficient of the glass component of the composite was measured to be 12.80×10^{-6} K^{-1}. The inter-tube space-corrected radial expansion coefficient of SWCNTs in the temperature region 300–800 K is known to be negative and has the value [16] -7×10^{-6} K^{-1}. Calculation of the volume strain of the SWCNTs/SWCNT bundles of the composite yielded a value $(\Delta V/V) \approx -0.022$. As the bulk modulus of SWCNTs is reported to be

35 GPa [17], the value of the compressive stress in the composite should be ~0.77 GPa. Thus, the SWCNTs in the composite are subjected to a compressive stress from all its circumferential sides and hence suffer from strains such as polygonization and radial compression. Ijima et al. [18] studied in detail stress-induced polygonization of 1.4-nm-diameter SWCNTs and calculated a compressibility factor for such tubes $(1/V)dV/P = 0.024\ \text{GPa}^{-1}$. Calculation of the compressibility factor of the SWCNTs (d = 1.3–1.5 nm) of the present composite gave a value of $\sim 0.028\ \text{GPa}^{-1}$ which is in agreement with the value reported by Ijima et al. [18]. It is known from previous studies [6, 10] that hydrostatic compression of semiconducting SWCNTs always decreases the band gap of their E_{11} band which is independent of the nanotubes' chirality. A similar hydrostatic compression-induced change in the band-gap energy was also reported in the case of the E_{22} bands. The phenomenon of radial compression induced lowering of the band gaps of semiconducting SWCNTs has been explained by considering $\sigma^* - \pi^*$ hybridization effect occurring near the maximum curvature points of the compressed nanotubes. Internal stress-induced radial compression of the semiconducting SWCNTs of the composite is expected to cause a change in their band structure from large band-gap- to small band-gap-type semiconducting nanotubes, i.e., to quasimetallic type. Shrinkage of the glass, during the cooling cycle of the composite, is expected to inflict stress on the incorporated SWCNTs/SWCNT bundles also along their lengths. Such stress would generate strains such as axial compression, bending (clearly visible in the HRTEM image), bending-related axial stretching, and torsion in the SWCNTs/SWCNT bundles. All these deformations would also influence the band structure of the SWCNTs in the composite. We have analyzed the effect of these structural strains in the SWCNTs on their band structures by using Eq. (1) of Yang and Han [6]. The equation is based on Huckel π-electron tight-binding model. It relates the changes in band-gap energies (ΔE_{gap}) of different SWCNTs to the percentage of strain in their structure and is valid in the low strain regime.

$$\Delta E_{\text{gap}} = \text{sign}(2p+1)3t_0[(1+v)\sigma\cos 3\theta + \gamma \sin 3\theta] \tag{1}$$

where σ and γ are the uniaxial and torsional strains acting, respectively, along the axis and the circumference of the nanotube, t_0 = 2.7 eV, the tight binding overlap integral, v is the Poisson ratio of the nanotube ≈0.2, θ is the chiral angle of the nanotube, and $p = -1, 0, 1$, such that chiral indices n and m satisfy the condition $n - m = 3q + p$, q being an integer.

According to Eq. (1), the axial stretching in the range $(0 < \sigma < 1)$ % would induce changes in the band-gap energies of the nanotubes of our composite as follows: The armchair metallic nanotubes (10, 10), (11, 11) with $p = 0$ and $\theta = \pi/6$ would have no effect on their band structures, i.e., $\Delta E = 0$. For quasimetallic (18, 0) nanotubes with $p = 0$ and $\theta = 0$, ΔE = +ve, i.e., the band gap would increase. Similarly for semiconducting (19, 0) nanotubes ($p = 1$, $\theta = 0$), there will be an increase in the band gap, but the result is opposite in the case of (17, 0) semiconducting nanotubes ($p = -1$, $\theta = 0$). In a similar way, the effect of axial compression ($-\sigma$) on the nanotubes may be understood. Considering the effect of torsion

(γ), it is revealed that for both +ve and −ve torsion, the armchair (10, 10), (11, 11) metallic nanotubes should suffer positive change in their band-gap energies, while the quasimetallic (18, 0) nanotube will have no effect on its band gap. Semiconducting (19, 0) and (17, 0) nanotubes should also remain unaffected. The nanotubes of other possible chiralities in the composite should also suffer changes in their band-gap energies under different strains depending on their respective chirality. Thus, in addition to the radial compression-induced quasimetallization of the SWCNTs, the above-described strains in the nanotubes will also affect their band structures as follows: (1) The first-order metallic bands of all metallic [(10, 10), (11, 11) armchair and quasimetallic (18, 0) zigzag] nanotubes would shift to higher energy; (2) semiconducting bands of (19, 0) zigzag nanotubes would shift to lower energy, but those of semiconducting (17, 0) zigzag nanotubes would have the opposite effect; and (3) the semiconducting bands of the nanotubes of other chiralities would experience shifts either to lower or higher energy depending on their individual chirality. The absorption spectrum of the SWCNTs of the composite, in fact, shows a significant shift of the averaged metallic band to higher energy compared to the energy of the metallic band of the pristine SWCNT-film. It also exhibits splitting of the S_{11} band into multiple bands, appearing both at lower and higher energy compared to the energy of the observed S_{11} band of the film. In the case of the S_{22} band, a shift to lower energy has also been noted. A significant modulation of band structure of the SWCNTs in the composite is thus evident.

To see the effect of band structure modulation of the SWCNTs of the composite on its electronic conduction, we have studied the *(I–V)* characteristics of the composite compared to that of the SWCNT-film. The *(I–V)* characteristics of the base glass have also been measured. These are shown in Fig. 3.

Three important features noted in the conduction behavior of the composite are as follows: (1) The composite exhibits a non-Ohmic behavior in its electronic

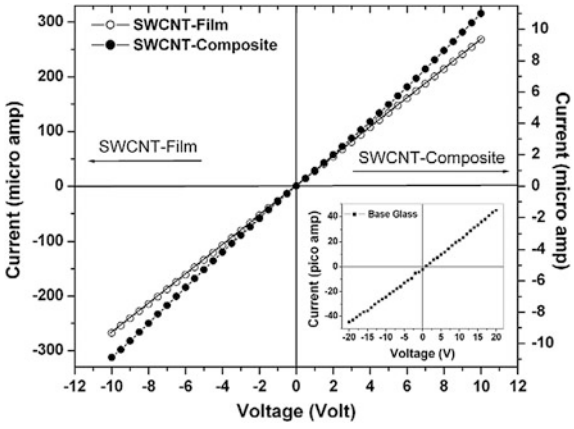

Fig. 3 *I–V* characteristics of the composite vis-a-vis that of the SWCNT-film. *Inset*: *I–V* characteristics of the base glass (after Ref. [5])

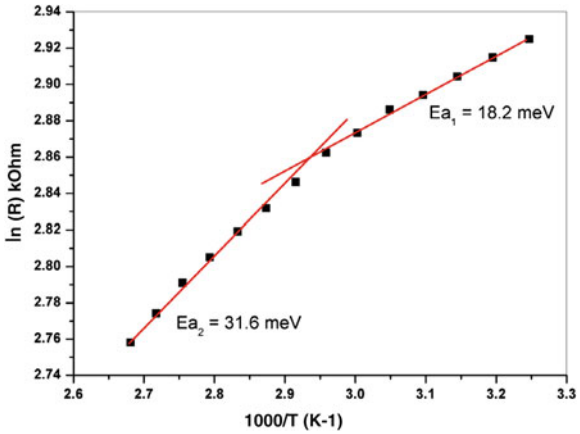

Fig. 4 Arrhenius plot of the temperature-dependent resistance data of the composite. E_{a1} and E_{a2} are activation energies of carriers flow (after Ref. [5])

conduction; (2) It carries only twenty times less current than that the SWCNT-film carries; (3) conductivity of the glass component of the composite, which is basically an insulator, increases a hundred thousand-fold after incorporation of the SWCNTs in its matrix. There is hardly any continuity among the dispersed SWCNTs of the composite; moreover, they are separated by layers of highly insulating host glass, and in spite of that, their current-carrying ability is reasonably good. The result, therefore, also indicates that the electronic conductivity of the SWCNTs of the composite has remarkably increased due to the modulation of their band structure from semiconducting to quasimetallic type. The Arrhenius plot of the temperature-dependent resistance properties of the composite is shown in Fig. 4. It shows two temperature regions of its conduction. In the low-temperature region (T = near room temperature), the resistance changes slowly with an activation energy $\sim$18 meV, while in the higher temperature limit, the resistance falls with a slightly faster rate showing an activation energy of $\sim$31 meV. A crossover temperature is noted in between 330 and 340 K.

The results of the absorption spectrum and the (I–V) characteristics of the SWCNTs of the composite have shown that the nanotubes of the composite at room temperature (300 K) exist with quasimetallic band structure due to their stress-induced structural deformations. With the increase of temperature because of its positive thermal expansion coefficient, the glass component of the composite should gradually expand and release its stress on its SWCNTs. However, out of the different stresses which the nanotubes experience in the glass, only the release of compressive stress would allow the nanotubes to expand to approach their original diameter. The other stresses such as torsion or bending will not make much difference because the composite, in this temperature range, still remains in the solid state. Because of the negative thermal expansion coefficient [16] of the SWCNTs, with the increase of temperature, a phenomenon of radial contraction of the nanotubes is also expected to occur. So the net radial expansion of the SWCNTs

will depend on the result of these two competing phenomena. It is obvious that with the increase of temperature, the compressed nanotubes of the composite may possibly suffer a slight increase in their diameters but would not be able to reach their original diameters. However, even a moderate net radial expansion of the compressed semiconducting nanotubes will increase their band-gap energies. This is definitely a factor that increases the activation energy of conduction of the SWCNTs of the composite (31 meV) in the higher temperature range.

Generally, a network of a pure SWCNT-mat contains nanotubes/bundles of nanotubes of different types, some of them are metallic and some are semiconducting, which may have various inter-tube contacts and intrinsic defects. Of the various possible contacts, only the 'semiconducting–semiconducting' and 'metallic–metallic' contacts create [19] good tunneling points, the others create barriers. Since most of the SWCNTs of the present composite are in a quasimetallic form, only one type of junction, namely quasimetallic–quasimetallic, is expected exist in the network of SWCNTs of the composite. Such junctions are expected to create good tunneling contacts. However, since the junctions in this case are separated by thin layers of the insulator glass, there will be a net increase in the resistance of the contacts, but the conduction mechanism [20] in the composite will remain unaltered.

Various series resistance models have been proposed to explain the electrical conduction properties of pure SWCNT-mats. Metallic and nonmetallic mixed conduction behavior of a SWCNT network is, however, best explained by the 'fluctuation-assisted tunneling conduction' model of Sheng [21]. In this model, the total resistivity (ρ) of a sample is taken as the result of series conduction between metallic islands separated by small tunneling barriers. Conductivity properties of a number of quasimetallic conducting polymers have been well explained by using the following modified version [22] of the above model:

$$\rho(T) = A\ \exp(-T_m/T) + B\ \exp[T_b/(T + T_s)] \tag{2}$$

where $\rho(T)$ is the resistance at temperature T. The first term on the right-hand side accounts for the quasi-1D metallic conduction with a characteristic energy $k_{\mathrm{B}}T_{\mathrm{m}}$, which accounts for the backscattering of the charge carriers. A and B are two constants which include the contributions related to the geometrical parameters. T_b is a measure of energy (k_BT_b) required for the charge carriers to tunnel through the barriers, and T_s/T_{b} is the quantum-induced tunneling in the absence of fluctuations and accounts for the decrease of conductivity at low temperature. A plot of resistivity versus temperature data of our composite is shown in Fig. 5.

The composite shows a small negative $\mathrm{d}\rho/\mathrm{d}T$ in the entire temperature range studied which also shows the quasimetallic characteristics of the nanotubes of the composite. Since the nanotubes of the composite exist with a quasimetallic band structure, Eq. (2) of the above model should be most suited to explain its conduction behavior. Interestingly, our experimental temperature-dependent resistance data of the composite fit excellently with Eq. (2). The fitted parameters T_b, T_s, and T_m obtained are 350, 332, and 1323 K, respectively. The energy required for charge carrier tunneling (k_BT_b) through the barriers of the composite was found to be

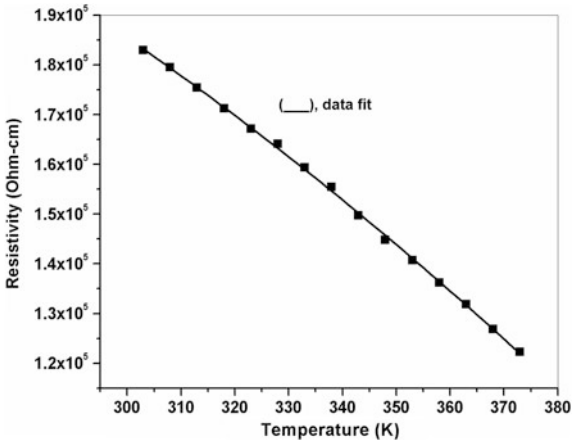

Fig. 5 Temperature versus resistance data plot of the composite and its fit to Eq. (2) (after Ref. [5])

30 meV, which is in excellent agreement with the value of the activation energy (∼31 meV) obtained from the Arrhenius plot. The value of the ratio (T_s/T_b) is ∼0.94, which is similar to the value (0.84) reported [23] for SWCNT/poly-(3-octylthiophene) composite with 8 % loading of the SWCNTs. The value of T_m = 1323 K is also of the same order of magnitude of the value (1,000 K) reported [24] for the metallic/nonmetallic SWCNT ropes. The excellent fit of the experimental data of the composite to Eq. (2) therefore suggests that the carrier transport in the composite above room temperature is dominated by the fluctuation-assisted tunneling, and the metallic component behaves like a quasi-1D metallic conductor.

3.2 *Photo-Induced Charge Separation in C_{60} or SWCNT/Glass Composites*

3.2.1 C_{60}/Glass Composite: Light-Induced Absorption (LIA) and Light-Induced ESR (LIESR) Studies

Steady-state absorption spectra of the C_{60}/(Pb)-phosphate glass composite recorded both before and after its UV–Vis irradiation as a function of time at 300 K, in the wavelength range 250–1250 nm are shown in Fig. 6, along with the similar absorption spectrum of the base glass both before and after its UV–Vis irradiation.

Prior to irradiation, the composite exhibits a weak and broad absorption band at ∼520 nm and a less distinct, broad band at ∼830 nm. Since the spectrum of the glass component of the composite does not show any absorption feature in this spectral region both before and after UV-irradiation, the observed absorption bands of the composite must be related to the C_{60} of the composite. Considering the

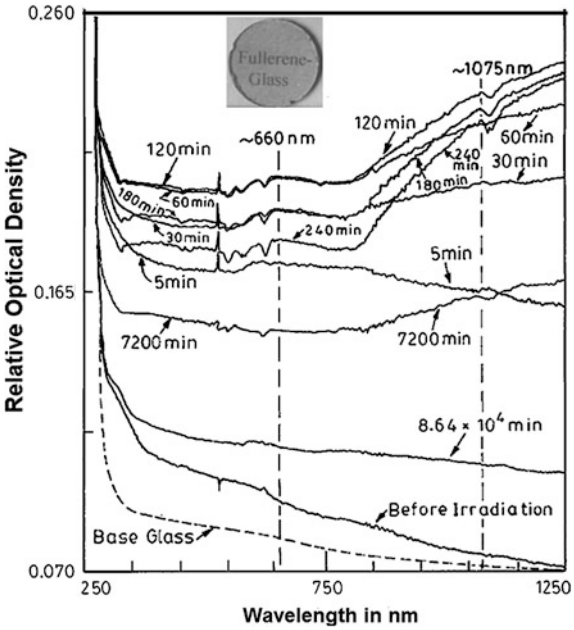

Fig. 6 Steady-state LIA spectra of a C_{60}-(zinc, lead) phosphate glass composite, as a function of time, (*Solid line*); Absorption spectrum of a similarly irradiated base glass as a function of time, (*Dashed line*). (Sample thickness, d = 0.2 cm in each case). A photograph of a polished transparent disc sample of the composite is shown in the Inset. Ref. [12]

energy and weakness of the 520-nm band, it can be safely assigned to the HOMO → LUMO forbidden transition of the C_{60} [25] of the composite. The 830-nm band, on the other hand, is most likely to originate from the C_{60} clusters [26] of the composite. Strong UV absorption of Pb^{2+} of the glass did not allow us to record any other high-energy absorption bands of C_{60} of the composite. It is mentioned above that the glass component of the composite does not show any photo-induced effect on its absorption due to irradiation. But surprisingly, the absorption spectra of the irradiated composite show a gradual emergence of a new broad absorption band around 1075 nm and enhancement in the absorption intensity around 660 nm.

The features of both the bands change continuously with time, showing a gradual increase in intensity and broadening in energy. The new bands attain an optimum intensity in $\sim$120 min. The absorption intensity thereafter starts falling and return, not exactly, but almost, to its pre-irradiation stage in $\sim 8.64 \times 10^4$ min. A plot of the absorption intensity (I) of the 1075-nm band versus time (t) (shown in Fig. 7) shows that its intensity grows exponentially with time.

An overall increase in the background absorption of the composite is also noted as a result of irradiation. To identify the active spectral region of the UV–Vis light, responsible for the above-described photo-effect, we have measured the absorption

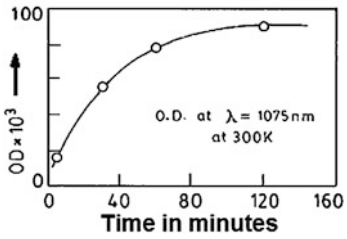

Fig. 7 Growth of fullerene-related anion concentration as a function of time (Ref. [12])

of composite irradiated exclusively with ultraviolet (230–400 nm) as well as irradiated exclusively with visible light (400–700 nm). In the case of irradiation only with visible light, no light-induced absorption (LIA) band was detected. Result thus showed that, although it was the ultraviolet light which was responsible for the photo-effect, simultaneous presence of visible light did not have any detrimental effect on the action of the UV light.

Concentrating to the origin of these two UV light-induced new absorption bands of fullerene, we find [27] that the $(C_{60})^-$ anion has two characteristic absorption bands: one $\sim$620 nm and the other $\sim$1070 nm, due to $^5t_u \rightarrow {}^8h_g$ and $^5t_u \rightarrow {}^2t_{1g}$ transitions, respectively. It is also known that in the case of the $(C_{60})^{n-}$ cluster anion, width of this 1070-nm band becomes broader. The observed UV-induced absorption band at $\sim$1075 nm and the increase in absorption intensity in the 660 nm region of the spectra of the irradiated composite thus show that both $(C_{60})^-$ and $(C_{60})^{n-}$ anions are formed in the composite due to UV irradiation.

The light-induced electron spin resonance (LIESR) spectrum of the UV-irradiated composite recorded at 300 K, two hours after the cessation of irradiation (time when the photo-induced absorption reaches a maximum), is shown in Fig. 8.

It exhibits two signals in the field region 275–345 mT. The lower field resonance is broad and has peak-to-peak width ΔH_{pp} = 9 mT and g = 2.27; the higher field

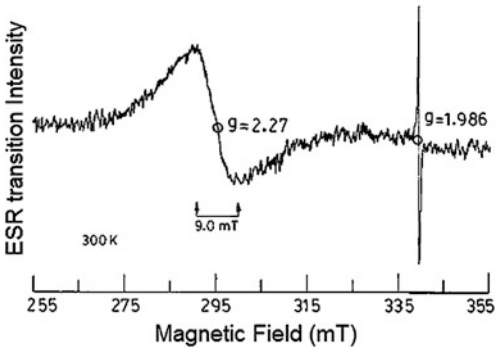

Fig. 8 Steady-state LIESR spectrum of the UV-irradiated C_{60}-(Zn, Pb) phosphate glass composite recorded 2 h after the cessation of irradiation, at 300 K. (Ref. [12])

resonance is sharp with a peak-to-peak width ΔH_{pp} = 0.3 mT and g = 1.986. The higher field signal can be attributed to UV-generated C_{60}-related anions. In the case of a C_{60} anion, g and ΔH_{pp} values are reported [27] to be in the range of 1.999–2.000 and 0.01–0.09 mT, respectively. The observed value of ΔH_{pp} in the present case (0.3 mT) is bit higher, and the value 'g' is slightly less compared to the respective reported values [27, 28] of an isolated C_{60} anion. However, such a lower value of g is not unusual because of the fact that the extra electron in the anion is largely delocalized. The observed broadening of the line width (ΔH_{pp}) is due to the formation of cluster $(C_{60})^{n-}$ anions. The values of the magnetic parameters (g = 2.27, ΔH_{pp} = 9.0 mT) of the lower field resonance, on the other hand, suggest that it should be associated with [11, 12] Pb^{3+} hole center (natural abundance of ^{204}Pb, ^{206}Pb, and ^{208}Pb together = 79 %; all of them have $I = 0$). Such hole centers are generated in the glass as a result of UV-induced hole trapping by the Pb^{2+} ions of the host. The photo-physical processes involved are as follows:

$$Pb^{2+} \xrightarrow{hv} Pb^{3+} + e \tag{3}$$

$$C_{60} + e \rightarrow C_{60}^{-} \tag{4}$$

$$(C_{60})_n + ne \rightarrow (C_{60})^{n-} \tag{5}$$

The photo-induced charge-separated state generated in this system was found to have an unusually long lifetime, indicating that immediate recombination of the carriers and holes is somehow inhibited. Another interesting phenomenon noted during the measurement of LIA as a function of time is that the fullerene anion formation in the system occurs few minutes after the irradiation, although light-induced hole trapping by Pb^{2+} ions of the system occurs instantaneously [11, 13]. This result indicates that the dynamics of formation of fullerene anions in the composite involve three steps: (i) Initially capturing of the electrons generated as a result of UV-induced hole trapping at the Pb^{2+} sites by some suitable trap within the glass structure; (ii) Release of these traps by the influence of the incorporated electrophilic fullerene and (iii) Finally their tunneling to the C_{60} and $(C_{60})_n$ sites to form the respective anions. Trapped electrons in a solid, which are stable in the absence of a scavenger, can get detrapped [29] in the presence of a scavenger. The probability that a trapped electron will survive at a time t in the presence of an electron scavenger of concentration C is given by the Eq. (6).

$$P(t) = \exp[-Cf(t)] \tag{6}$$

where $f(t) = \int [1 - \exp\{1 - tk(r)\}] 4\pi r^2 dr$, k(r) is the rate constant of transfer of the trap to the scavenger at a distance r.

According to Eq. 4, the trapped electron yield at a given concentration of fullerene in the glass should decrease exponentially with time, i.e., concentration of the detrapped electrons will increase exponentially with time, in other words the

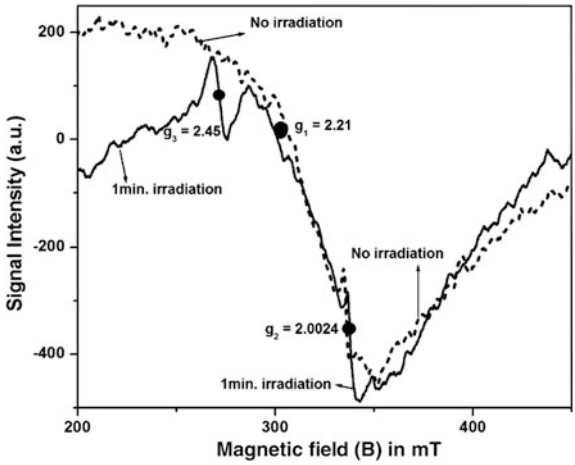

Fig. 9 ESR spectra of the composite with (*Solid line*) and without (*Dashed line*) illumination of UV–Vis light from a 150-W xenon lamp (after Ref. [5])

concentration of fullerene-related anion in the composite will increase exponentially with time. The rate of growth of concentration of the fullerene-related anion in the UV-irradiated composite as a function of time has been shown in Fig. 7. The observed exponential rate of growth of the fullerene-related anions is in good agreement with the Eq. (6).

3.2.2 SWCNT/Glass Composite

To check the possibility of light-induced charge separation in our *SWCNT/glass composite*, ESR spectra of the composite were studied with and without in situ illumination of UV–Vis light. These are shown in Fig. 9. The composite in the absence of light gives a spectrum, which exhibits a broad ESR signal with '*g*' tensor $g_1 = 2.21$ and a line width ΔH_{pp} (peak-to-peak) = 125 mT. Overlapping with this broad signal, a sharp signal with $g_2 = 2.0024$ and $\Delta H_{pp} = 2.8$ mT is also noted. The value of '*g*' tensor ($g_1 = 2.21$) and the line width of the broad signal suggest that the signal is associated with the paramagnetic Ni-nanoclusters [30] that were used by the manufacturer for the synthesis of the SWCNT product of our study. This proposition is supported by the manufacturer's documented specifications of the material (Aldrich, product No 652490). It is well known that the ferromagnetic catalysts normally used for the synthesis of SWCNTs always remain as a contaminant with the product. These impurities cannot be removed from the sample even after soft-bake acid purification. The value of the *g* tensor ($g_2 = 2.0024$) and the narrow line width ($\Delta H_{pp} = 2.8$ mT) of the overlapping sharp signal, on the other hand, suggests that the signal should be associated with the surface-lying conduction electrons of the SWCNTs [31, 32].

Upon UV–Vis light illumination, the composite exhibits a dramatic change in its ESR spectrum. Within a moment of illumination, the intensity of the signal due to conduction electrons of the SWCNTs becomes almost double of its dark value, directly showing that the SWCNTs of the composite gain in the population of their conduction electrons due to UV–Vis illumination. Concomitant with the above, a new signal with g tensor (g_3 = 2.45) and line width ΔH_{pp} = 9 mT appears in the low-field region of the spectrum. The values of the magnetic parameters of the new signal (g_3 = 2.45 and ΔH_{pp} = 9 mT) in this case also indicate that the signal owes its origin to Pb^{3+} holes, which are generated in the system as a result of UV–Vis irradiation [11, 12].

The observed phenomenon of enhancement of the intensity of the signal due to conduction electrons of the SWCNTs upon UV–Vis light illumination, on the other hand, suggests that the irradiation-generated electrons are captured by the SWCNTs. The related photo-induced reactions may be written as follows:

$$\mathrm{nPb}^{2+} \xrightarrow{\mathrm{nh}\nu} \mathrm{nPb}^{3+} + \mathrm{n}e,$$

$$(\mathrm{SWCNT})_{\mathrm{m}} + \mathrm{n}e \rightarrow (\mathrm{SWCNT})_{m}^{\mathrm{ne}}$$

The process of capture of the photo-generated electrons by the SWCNTs was found to reach a saturation level soon, and thereafter, no light-induced increase in the intensity of the signal of the conduction electron is observed. This result indicates that the light-induced forward electron transfer from interstitial Pb^{2+} ions to the neighboring SWCNTs and its back-transfer reach equilibrium within a short time and an equilibrated charge-separated state is created in the system [9].

The observed phenomenon of attaining saturation in the process of capturing of the photo-generated electrons by the SWCNTs encouraged us to check whether such capturing process by the SWCNTs can be made continuous by continuous draining out the captured electrons from the SWCNTs by applying a suitable bias. So we have studied the conduction properties of the composite as a function of applied bias with and without illumination of the UV–Vis light in air. Since pristine SWCNT is also known to be sensitive to the UV and near visible radiation [32, 33], the electrical properties of the SWCNT-mat were also studied in air side by side, under similar illumination conditions. All these results are shown in Fig. 10a, b.

In the absence of illumination, the conductivity (S) of the pristine SWCNT-mat remains more or less constant at the initial stage of increase in the applied voltage; thereafter, the conductivity increases steadily with the increase in voltage. Under the illumination of UV–Vis light, it shows a reverse trend, i.e., the conductivity decreases steadily from the very beginning with the increase in the applied voltage (Fig. 10a). It is already known [33, 34] that adsorption and desorption of oxygen on or from the surface of SWCNTs may have profound effect on the electronic properties of SWCNTs. Phenomenon of light-induced desorption of O_2 from the surface of SWCNTs is also known. It has been shown that the conductance of SWCNTs decreases due to the light-induced desorption of oxygen from the surface

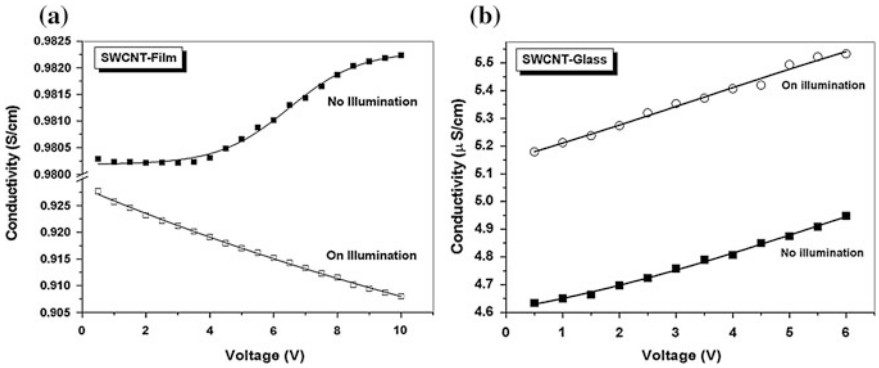

Fig. 10 **a** Electrical conduction properties of the pristine SWCNT-mat in air with and without illumination. **b** The same of the composite in air with and without illumination

of the SWCNT-film and regains the value on re-adsorption of O_2 from air in the dark. The observed decrease in conductance of our SWCNT-mat in air under UV–Vis light illumination is the effect of light-induced O_2 desorption from the surface of the SWCNT-mat. In the case of photo-induced electronic properties of the SWCNT-composite, it is observed that the composite in air and in the absence of UV–Vis light shows a linear increase in conductance with the increase in the applied bias from the very beginning (Fig. 10b). Under UV–Vis illumination, it shows an abrupt initial increase in its conductance at the starting bias, which thereafter gradually increases linearly with the increase of voltage. The results clearly show that the conduction behavior of the SWCNTs of the composite is quite different from that of the SWCNTs of the mat both in the presence and absence of UV–Vis illumination. The result also indicates that the glass component of the composite has some definite role in changing the conduction property of the SWCNTs of the composite. As shown earlier, that SWCNTs in this composite exist with a 'quasimetallic' band structure because of the host-related stress-induced structural deformations. This metallization effect of the SWCNTs in the composite has definitely helped the latter to conduct current more efficiently than the pristine SWCNT-mat even in the absence of any illumination. Since the phenomenon of O_2 adsorption and light-induced O_2 desorption on and from the surface of the SWCNTs are not possible in the case of the composite, the observed abrupt increase in conductivity of the composite under UV–Vis light illumination must be due to some other photo-induced effect. It is known from our ESR studies that UV–Vis irradiation of the composite generates Pb^{3+} holes in the system by dislodging electrons from the interstitial Pb^{2+} centers of the glass, and the photo-generated electrons thus formed are captured by the neighboring SWCNTs showing an increase in the population of their conduction electrons and the process reaches equilibrium within a short time. When a bias is applied across the composite, these captured electrons are drained out of the SWCNTs to flow into the outer circuit showing an abrupt increase in the conductivity. The moment some of the captured

electrons of the SWCNTs are drained out by the applied bias, the equilibrium is disturbed and the SWCNTs start capturing a fresh lot of photo-generated electrons. Constant application of voltage thus helps the SWCNTs of the irradiated composite to continue the process of capturing of photo-generated electrons maintaining a high level of conductivity. Such a phenomenon is potential for use in photo → current conversion.

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Novel Nanostructured Passives for RF and Power Applications: Nanopackaging with Passive Components

P. Markondeya Raj, Parthasarathi Chakraborti, Dibyajat Mishra, Himani Sharma, Saumya Gandhi, Srikrishna Sitaraman and Rao Tummala

Abstract Miniaturization of passive components, while mounting them close to the active devices to form ultrathin high-performance power and RF modules, is a key enabler for next-generation multifunctional miniaturized systems. Traditional microscale materials do not lead to adequate enhancement in volumetric densities to miniaturize passive components as thin films or thin integrated passive devices. With these materials, component miniaturization also degrades performance metrics such as quality factor, leakage current, tolerance, and stability. Nanomaterials such as nanocomposite dielectrics and magneto-dielectrics, nanostructured electrodes, and the resulting thin-film components have the potential to address this challenge. This chapter describes the key opportunities in nanomaterials and nanostructures for power and RF passive components. The first part of this chapter describes the role of nanostructured materials for high-density capacitors and inductors in power modules. The second part of the chapter describes application of nanoscale materials as nanocomposite dielectrics and magneto-dielectrics with stable and high permeability and permittivity for miniaturized RF modules.

1 Introduction

Passive components are required in an electronic system for providing various power functions such as decoupling and voltage conversion, and RF functions such as filters, matching networks, resonators, and EMI isolation. The primary drivers for passive component evolution over the past few decades have been thickness reduction by enhancing properties and processing as thinner films and also provide

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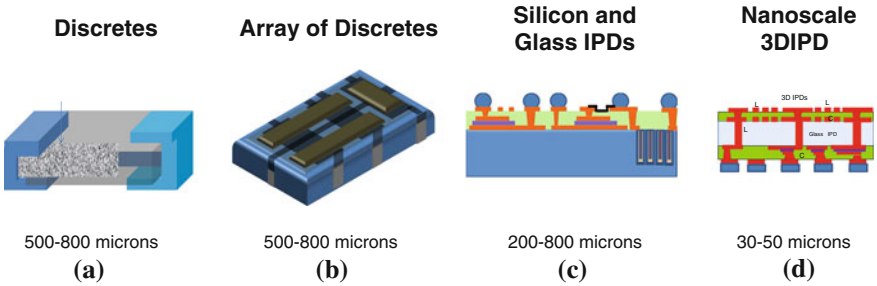

Fig. 1 Evolution of passive components from discretes to integrated passive devices (IPDs) and 3D IPDs

proximity to the active devices that they serve to provide these functions. These drivers have resulted in a continuous reduction in passive component thickness from 0.5 mm in the past to 0.15–0.3 mm with standards of 0201 and 01005 s, as shown in Fig. 1a, resulting in module thicknesses with passive and active components of ~1 mm. As these components are large and are mounted far from the active ICs, they add parasitics that scale with interconnection length and deteriorate the module performance [1].

Recent advances from discrete component manufacturers have enabled components of 100 micron thickness [2]. Such ultrathin passives have led industry to embed such discrete passives in the package buildup layers [3, 4] or assembled on the back of the package. This approach substantially reduces the package thickness and the distance to active devices to less than 200 microns, improves the module performance, and saves the package and board space. This approach is, however, limited by the component thickness (0.15–0.5 mm) and the number of components.

Passive arrays and integrated passive devices (IPDs) have evolved as an alternative approach to reduce the component count, footprint, and interconnect parasitics, as shown in Fig. 1b, c. IPDs with low-temperature cofired ceramics (LTCC) achieve the highest quality factors (Q) at GHz frequencies for RF interconnects and components, but cannot meet the reduced thickness needs. Silicon IPDs [5–7] (Fig. 1c) show high losses and do not meet the Q requirements for high-performance RF applications. Passive-integrated silicon substrates received more attention for power components as high-density capacitors or high-density inductors on silicon [8]. However, the limited properties and use of expensive semiconductor processes have been a major constraint in wider acceptance of this technology. Thin-film RF components are now being integrated onto glass substrates for enhanced Q and miniaturization [9]. These IPDs are fabricated on thick glass as one-sided components and are surface-mounted on the board as passive modules.

As the ultimate goal in system miniaturization and performance enhancement, institutes such as Georgia Tech. PRC and its industry partners, and semiconductor and packaging companies have advanced R&D in embedded thin-film passive technologies for the past two decades. The objective here is to integrate the passives

as thin-film layers in the package buildup layers or in the ICs. However, embedded thin-film passives face several unresolved manufacturing issues related to achieving adequate capacitance and inductance densities, precision, testability, reworkability, and defect-driven yield losses.

Because of the manufacturing limitations with IPDs and embedded passives, functional modules in today's systems are predominantly made of discrete thick active and passive components that are connected with each other through a thick interconnect substrate with coarse-pitch surface-mount technology (SMT) interconnections. The overall impact of advances in active component to nanoscale on system size and performance is, therefore, limited by the passives that are mounted far away from the active components on thick organic or ceramic module substrate.

Nanomaterials provide several opportunities for simultaneous miniaturization and performance enhancement in power and RF passive components. The key requirements for emerging passive components are listed in Table 1. The table also shows examples of nanomaterials and nanostructures to meet these component requirements. Nanostructured materials result in 5–10× miniaturization in energy storage components for power components. They also alleviate the process compatibility issues, allowing multiple components to be integrated on a single glass substrate. Nanomaterials show superior electrical properties for capacitors and thus lead to miniaturized high-Q multilayer passives with higher dielectric constant and low TCC, wideband, and low-loss interconnects. They also show superior magnetic properties from improved exchange coupling between the domains, absence of leakage, absence of domain wall-assisted relaxation, etc. These nanostructures are expected to result in higher permittivity and permeability at much higher frequencies as compared to the current materials, leading to reduction in size and improved performance [10, 11] in board-compatible embedded antennas,

Table 1 Nanomaterials and nanostructures for passive component applications

	Properties	Nanomaterials and nanostructures
Power inductors	• Low coercivity: <0.1 Oe • High permeability: >100 • Loss tangent: <0.01 • Frequency stability: 10–100 MHz	• Metal nanocomposites • Nanogranular materials • Nanostructured ferrites
Power capacitors	• Volumetric density: >100 uF/mm^3 • ESR: <25 milliohms × μF • Leakage current: <10 nA/μF	• Nanoelectrodes; • Conformal nanoscale dielectrics
RF inductors	• $\mu_r > 5$ • Stability >1–10 GHz • Q > 100	• Metal nanocomposites; • Nanoscale hexaferrites
RF capacitors	• TCC: 30 ppm/C • Permittivity >20	• Nanocomposites • High-K super paraelectric fillers
Antennas	• $\mu_r \times \varepsilon_r > 10$; • $\mu_r/\varepsilon_r > 0.5$	• Metal nanocomposites; • Nanoscale hexaferrites
EMI isolation	• −60 dB isolation	• Metal nanocomposites

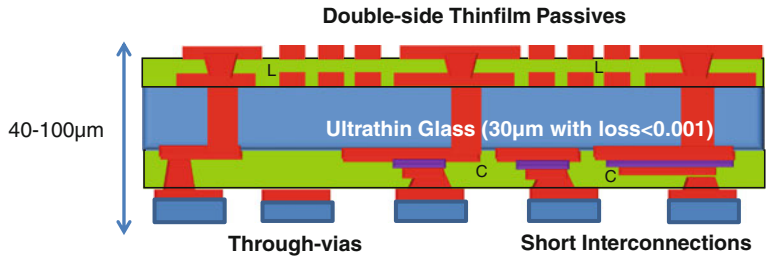

Fig. 2 3D IPD concept for power and RF applications

reconfigurable modules using MEMS, and nanostructured electronic band gap structures for RF-digital noise isolation. The need for nanomaterials in RF modules as capacitors, inductors, and antennas is compiled in the last four rows of Table 1.

2 Nanoscale 3D Integrated Passive Devices (3D IPDs)

Nanoscale passives combine the benefits of advanced thin-film passives with superior properties, thickness reduction with double-side components from through-vias, and mounted or surface-assembled with ultrashort interconnections on a thin substrate, evolving into a new class of 3D integrated passive devices or 3D IPDs. The schematic 3D IPDs for RF applications are shown in Fig. 2. In a RF 3D IPD, high precision and high-Q inductors and capacitors are formed on a through-via glass substrate with thin-film buildup layers. Similarly, power 3D IPDs can also comprise of high-density power inductors and capacitors, and thin-film capacitors on a thin glass substrate with through-vias. In terms of passive component integration, 3D IPDs go beyond the state of the art in many ways—novel thin-film materials and processes for higher volumetric density; quality factor and voltage, frequency, or thermal stability; ultraminiaturized and testable RF; and high-performance module by virtue of closest proximity between actives and passives.

These 3D IPDs, in turn, result in ultrathin 3D integrated passive and active component (3D IPAC) functional modules with 3–5× reduction in size and 2× reduction in cost compared to today's bulky discrete functional modules [12].

3 Nanoscale Power Components

3.1 Power Inductors

Thin-film inductors require magnetic cores with higher permeability, field anisotropy, low coercivity, and frequency stability. Today's magnetic materials for power

inductors face several shortcomings toward these requirements. Even though ferromagnetism, which is a well-known phenomenon that results in high permeability and high saturation magnetization, exists in metals such as Co, Fe, and Ni, these are not suitable for high-frequency applications because of their high electrical conductivity that leads to eddy current losses. Ferrites are based on oxides of these metals and have higher electrical resistivity, thereby being more suitable for power inductor applications. Spinel ferrites (e.g., $NiFe_2O_4$, Mn–Zn and Ni–Zn ferrites) [13, 14] are extensively used in power converters because of their lower losses than metal cores, resulting in high-Q factors at moderate frequencies of 100 kHz–1 MHz. However, for emerging high-frequency consumer applications, ferrites suffer from several major disadvantages, including low saturation magnetization and poor frequency response of magnetic properties due to their strong relaxation behavior. These limitations lead to millimeter size components and thus make ferrites unsuitable for emerging applications.

Metal–polymer composites, in contrast, can address this problem because of their higher saturation magnetization while retaining higher resistivity. These composites consist of metallic magnetic particles that are coated (or separated) by an insulating phase. Such magnetic powders in polymer paste form are commercially available from various vendors. Examples of these include iron and permalloy powders, which show permeabilities of 40–100 in the low MHz frequency range [15]. However, these materials show insufficient permeabilities and unstable properties beyond 10 MHz, which limits them to lower frequency applications only.

Magnetic nanocomposite materials are comprised of nanoscale magnetic particles in an amorphous matrix. Such materials provide unique opportunities to address the fundamental limitations of traditional magnetic materials, as shown in Fig. 3. Higher permeability in magnetic nanocomposites at microwave frequencies can be achieved by reducing the particle size and the separation between neighboring metal particles down to the nanoscale, which leads to novel magnetic exchange coupling phenomena [16]. For example, Co- or Fe-based nanocomposites show much higher permeability and frequency stability at microwave frequencies than those obtained from the bulk Co or Fe metal or their microscale composites [17]. The exchange coupling interaction, which is attributed to the magnetic ordering within grains, also extends to neighboring grains within a characteristic

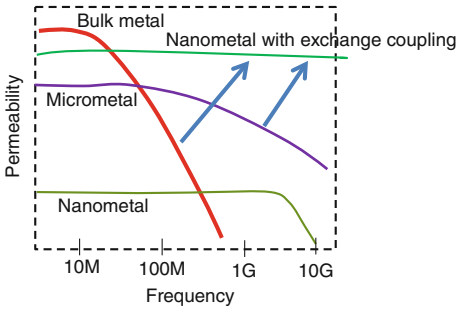

Fig. 3 Nanomagnetic composite structure and its benefits

distance, l_{ex} [18]. The exchange interaction in nanocomposites also leads to the cancelation of magnetic anisotropy of individual particles and the demagnetizing effect, leading to improved soft magnetic properties [17]. Because of the nanosized metal particles, the eddy currents produced within the particle are also negligibly small, leading to much lower loss for nanocomposites, compared to that of conventional microsized ferrites and powder materials.

Magnetic cores with sputtered high-resistivity nanogranular alloys such as Co–Zr–Ta, Co–Hf–Ta–Pd, and Co–Zr–Nb can increase the frequency stability and quality factor. Inductors displaying 0.05–0.15 μH/mm^2 at 1–2 MHz [19, 20] are reported with such cores. On the other hand, in the pioneering work by Intel on on-chip power inductors, nanolaminates with spiral coils showed inductance densities of up to 2.0 μH/mm^2 at 500–1000 MHz, 10× higher than the state of the art [21]. Their work demonstrated that nanolaminates can increase the roll-off frequency from 300 to 800 MHz. These inductors take advantage of the uniaxial magneto-crystalline anisotropy in the magnetic core surrounding the spiral inductor coils. However, the power handling with these inductors is limited unless the inductor thickness is increased to several microns, which requires new innovations in nanomagnetic synthesis.

3.2 Power Capacitors

Multifunctional systems for mobile and high-performance computing typically operate with multiple power rails on multiple voltage levels. Capacitors are widely employed for voltage conversion and ripple-free voltage supply over a broad frequency range. In a typical power distribution network (PDN), multiple capacitors are incorporated at different levels of the system to provide the decoupling function. Today's discrete capacitors can only address decoupling needs in a narrow frequency band. This typically increases the number of discrete capacitors, thus the package size, and also limits the high-frequency performance. The trend to capacitor array with multiple components can address this challenge to some extent by patterning the capacitors into multiple sizes but presents other limitations related to thickness, cost, proximity to active devices, and other design constraints from the low capacitance densities.

The volumetric density of available discrete capacitors has not caught up with the demand for high-density capacitors in integrated thin power modules. This is because of several fundamental limitations with existing capacitor technologies. The capacitance density is directly dependent on the electrode surface area, dielectric permittivity, and thickness. Today's high-density capacitor technologies suffer either from low surface area because of the microscale electrodes or from low permittivity of dielectrics, or both. Tantalum capacitor technologies provide high surface area enhancement, but the dielectrics are limited to tantalum pentoxide with a permittivity of about 25 [22, 23]. With nanoscale tantalum electrodes, the capacitance volumetric density can be further increased but degrades the equivalent

series resistance (ESR) and frequency stability. On the other hand, multilayered ceramic capacitors (MLCC) do not have adequate area enhancement because of limitations of ceramic and metal thick-film technology [24]. The trend toward silicon trench capacitors provides limited area enhancement because of the limitations of silicon micromachining technologies. Conformal coatings with atomic layer deposition (ALD) on such deep trenches are another major challenge [25, 26], while thermal oxidation or nitridation limits the dielectrics to lower permittivity values.

Nanoparticle electrodes provide much high surface area compared to trench capacitors and are currently being developed to improve the capacitance density by a factor of 10× at lower cost using scalable materials, tools, and processes. [27]. The porous electrodes with partially sintered nanoparticles provide ultrahigh surface area per unit volume resulting in area enhancement of above 1000× for a 50 micron thick film. Capacitance densities of above 400 $\mu F/cm^2$ have been demonstrated with breakdown voltages exceeding 15 V for a component thickness of 50–70 microns [28].

The capacitance density can be further improved with ultrathin dielectrics of 20–30 nm. High capacitance density with nanoscale dielectrics usually leads to high leakage current in a capacitor which is detrimental to its performance and reliability. This can be addressed by using conformal and uniform or self-limiting dielectric with least defect density. A conformal and uniform dielectric deposition can be achieved using ALD. However, ALD is an expensive process with high deposition time and low throughput, particularly with porous electrodes that require long diffusion times. On the other hand, nanoelectrodes using valve metals can be readily oxidized by immersing the nanoelectrodes in an electrolytic bath while subjecting the nanoelectrode to a potential bias. This process is known as anodization and has been widely used in the electrolytic aluminum and tantalum industry.

Leakage current can be further minimized by using self-healing cathodes. The self-healing works on the principle of isolating the cathode next to the defect site in the dielectric such that no current flows through the site thus preventing a short. Manganese oxide (MnO_2) and conductive polymers such as PEDOT:PSS are the most widely used self-healing cathodes in the tantalum capacitor industry. MnO_2 is formed by dipping the dielectric-coated high surface area electrodes into an aqueous manganese nitrate ($Mn(NO_3)_2$) solution followed by thermal annealing. Multiple impregnations and annealing cycles are employed for conformal MnO_2 coating over the high surface area architecture. However, MnO_2 has a lower conductivity ($\sim$10 S/cm) than PEDOT:PSS ($\sim$100–600 S/cm) leading to higher electrode resistance and ESR, as compared to polymer-based capacitors.

ESR in MnO_2 can be lowered by carefully controlling the oxygen levels during the reaction to prevent the formation of resistive manganese oxide (Mn_2O_3). This leads to the formation of dense, smooth, and uniform manganese dioxide layers with higher electrical conductivity. Introduction of oxidizing agents such as nitric acid, hydrogen peroxide, and ozone during the annealing of $Mn(NO_3)_2$ was explored for forming highly conductive and conformal MnO_2 layer with lower ESR [29].

Use of alternative organic polymers such as thiophene-based PEDOT, with higher conductivity, better ESR, and ease of processibility, is being actively used in tantalum capacitor industry. Conducting polymer such as poly (3-hexylthiophene-2,5-diyl) or P3HT is another potential candidate that could be explored for use as cathode. The conductivity of P3HT is in the range of $\sim 10^3$ S/cm, which could be further enhanced by the addition of endometallo fullerene or phenyl-C61-butyric acid methyl ester (PCBM) [30, 31]. However, the self-healing capabilities of P3HT as a cathode are still a subject of investigation for the researchers.

GT-PRC has recently demonstrated novel approaches for integrating nano-structured electrodes and conformal nanoscale dielectrics on silicon or non-silicon substrates leading to ultrathin capacitors. The first approach involves low-temperature sintering of base metals such as copper directly on silicon to form porous copper electrodes as anodes. Alumina is conformally deposited over the porous copper electrodes using the process of ALD followed by dispensing of conducting polymer as cathode [32]. In the second approach, etched valve metal foils were evaluated as a high surface area electrode, followed by anodization process for dielectric deposition. The electrochemically etched Al foils with high aspect ratio of above 50 were anodized to form conformal, thin aluminum oxide dielectric. In both the approaches, PEDOT:PSS was used as the cathode material which was coated conformally using simple solution dispensing methods. High surface nanoscale tantalum electrodes were also integrated on silicon substrates as an alternative anode structure. The advances have shown capacitance densities of 100 μF/cm^2 using silicon or package-compatible processes. The approaches are schematically illustrated in Fig. 4.

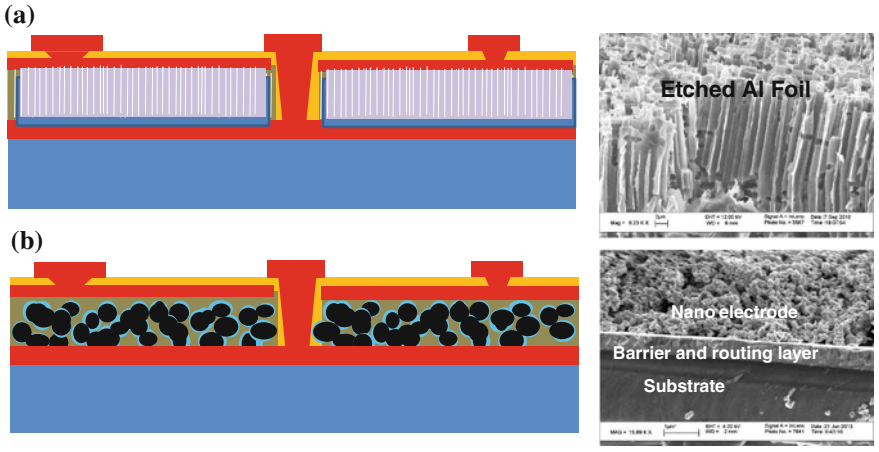

Fig. 4 Two approaches for integrating high-density nanocapacitors in 3D IPDs. **a** Etch foil. **b** Nanoparticle electrode

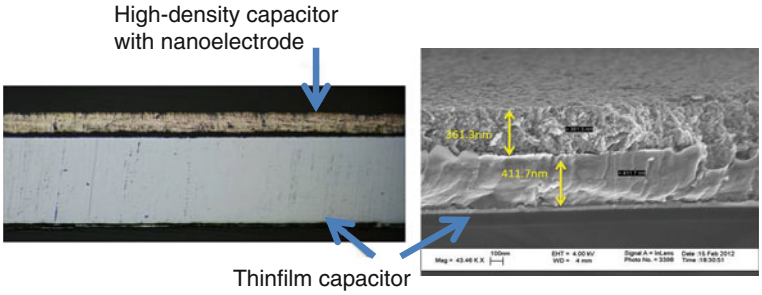

Fig. 5 3D IPD with high-density and thin-film decoupling capacitors

Several advances have been made in integrating thin-film decoupling capacitors [33, 34] for more than a decade. These include high-K dielectrics with silicon, glass, or organic substrate-compatible processes for high-permittivity films both as ceramic thin films and ceramic–polymer composites. The 3D IPD capacitor approach takes these thin-film capacitors and high-density nanostructured capacitors further by integrating them on a single substrate with through-vias. The 3D IPD capacitor network will have nanoelectrode capacitors (1 μF/mm^2) on one side for decoupling at low–mid frequencies and high-permittivity thin-film capacitors (20–30 nF/mm^2) on the other side at higher frequency bands, as illustrated in Fig. 5. Further, it gives better performance than embedded thin-film decoupling capacitors because of the close proximity (<40 microns) between the active and 3D IPD passives, as shown in Fig. 2. The devices can be tested before assembling on the 3D IPAC substrate. Advanced glass-based 3D IPDs with high dielectric constant thin films using glass-compatible processes have been developed [35, 36] to achieve this goal.

4 Nanoscale RF Components

4.1 RF Capacitors

Miniaturization of RF components such as filters, oscillators, matching networks in amplifiers, and antennas, operating with high performance at GHz frequencies, needs materials with higher permittivity and permeability, along with stringent tolerance in dielectric and magnetic properties, low temperature coefficient of permittivity (TCK), and low-loss tangent (Df). Over the past few decades, high-frequency components were therefore mostly confined to thick-film LTCC, owing to its low loss, stable properties, and partial integration capability, although the end-systems were bulky and costly [37, 38]. Polymer dielectrics, on the other hand, provide the benefits of low-cost manufacturing and the capability to integrate completely with the rest of the polymer-based system. RF components from low-loss polymers such as liquid crystal polymer (LCP), bisbenzocyclobutene (BCB), and polytetrafluoroethylene (PTFE) are now integrated to meet the stringent

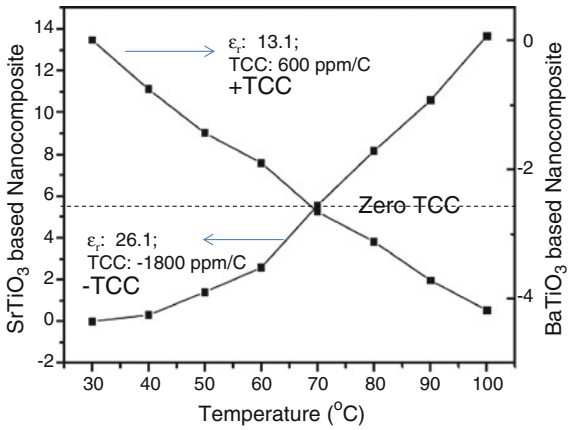

Fig. 6 Nanostructured dielectrics with high-K and low loss, but with opposite TCC, that can be used for compensation

requirements of high-performance systems. The low dielectric constant of such materials, however, leads to relatively larger component designs and is a major barrier for miniaturization and performance of wireless interfaces. Several substrate companies are now focusing on developing novel RF substrates by incorporating low-loss paraelectric-like high-K fillers in PTFE-based materials. These high-K and low-loss RF substrates are good candidates for miniaturizing certain RF circuits. However, they do not meet the temperature coefficient of capacitance (TCC) and low-loss requirements for several other applications. Any increase in the dielectric constant is accompanied by a strong dependence of capacitance with temperature, frequency, voltage bias, and film thickness.

For miniaturized RF components, nanocomposite materials based on nanostructured superparaelectrics provide new avenues for high permittivity, low loss, frequency stability, and low TCC [39]. Ferroelectrics at nanoscale show linear permittivity behavior with temperature, but with either +TCK or −TCK depending on the phase transition temperatures. These fillers can be used to effectively compensate the net TCC as illustrated in Fig. 6. By incorporating paraelectric fillers into the low-loss buildup layers, composites with permittivity 3–4× higher than the polymer matrix have been achieved with low TCC [40] even with traditional organic buildup layers. Novel high-K thin-film RF dielectrics based on glass-compatible nanostructured superparaelectrics that can enhance the permittivity without compromising stability and loss [41] are now being developed.

4.2 RF Inductors

Major fundamental and technological advances in the design and fabrication of high-frequency inductors have been demonstrated [42]. In combination with

low-loss polymer buildup dielectrics (dielectric loss of 0.002) and polymer core substrates, multilayered inductor structures can be built without significant degradation in Q. RF inductor design libraries for high-density, Q of above 200, and self-resonant frequency (SRF) of above 10 GHz were built with various substrate geometries and design rules. Glass is a much superior material for high inductance density and Q because it combines the benefits of (a) ceramics for ultralow loss, (b) organics for large-area and low-cost processing, and (c) silicon for high density and precision coil definition. Planar spiral inductors designed with sufficient distance from the ground planes resulted in an inductance density of 50 nH/mm^2 and Q of above 60 on glass substrates [43]. Higher inductance density without compromising losses from the coil resistance, however, remains to be achieved.

For higher inductance densities with high Q, low-loss and high-permeability dielectrics are desired. However, magneto-dielectrics with stable permeability and low loss in GHz frequencies are not currently available. Magnetic materials suffer from eddy current and domain wall losses, which make them unsuitable for frequencies above 100 MHz. To enhance frequency stability, the materials should have single-domain nanosize particles with suppressed eddy current and domain wall losses. However, such materials usually show low permeabilities unless the nanoparticles are densely packed to enable exchange coupling between them. The frequency stability of permeability with micro- and nanoscale materials is schematically illustrated in Fig. 7. Nanogranular materials or nanoscale thin films have been shown to have frequency stability with permeabilities of above 100 [44, 45]. These materials will find applications in RF inductors in thin film form because of their low-temperature sputter processing that is compatible with large glass panels.

Certain hexaferrites are also emerging as promising candidates for high-frequency applications [46]. These materials show high crystal field anisotropy leading to high FMR, with the combined advantage of low eddy current losses. The large particle size during ferrite processing at high temperatures, however, leads to

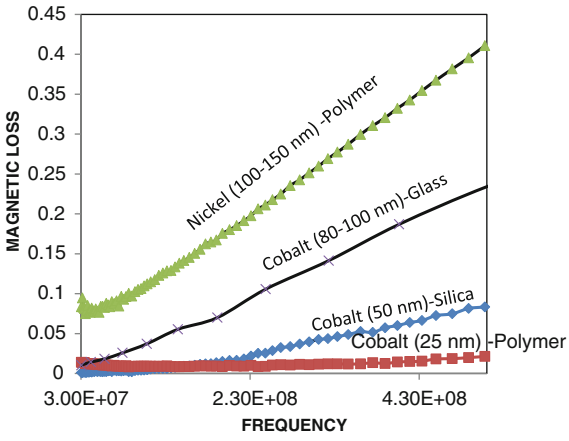

Fig. 7 Role of nanostructured materials in frequency stability

higher losses and instabilities presumably from domains. Efforts to suppress grain size with glass additives were shown to yield lower loss in 2–3 GHz range [47].

4.3 Filters

Filters from 3D IPDs with double-side inductor and capacitor components, going beyond today's silicon IPDs in improving the performance and component density, were recently demonstrated [43, 48]. The ultralow dielectric loss in glass enables the highest quality factors, superior to that of ceramic or organic modules, but with much higher integration and component density, low substrate and interconnect loss, at low cost. Through-via formation using low-cost packaging tools and processes such as laser vias and wet metallization techniques was utilized for interconnecting the components on both sides. Typical second-order filters show an insertion loss of less than 1 dB and return loss of above 25 dB. With the potential advances in nanoscale dielectrics and magneto-dielectrics described in Sects. 4.1 and 4.2, much superior performance and miniaturization are anticipated in the future.

4.4 Antennas

Antenna size has been a major bottleneck for reducing the size of RF front-end modules. The antenna dimensions are proportional to $1/\sqrt{\varepsilon\mu}$. The antenna size can be reduced by surrounding it with a material of either high permittivity (ε) or permeability (μ), thus leading to miniaturized designs. Thin antennas, however, suffer from relatively narrow bandwidth, substrate dielectric loss, mutual coupling with their substrate, and surface wave perturbation issues [10].

Nanoscale magnetic composites offer both higher permittivity and permeability and therefore offer superior antenna performance as measured by bandwidth and gain while also allowing miniaturization. Metal–polymer nanocomposites with both high permittivity and permeability for miniaturizing antennas have been studied by GT-PRC [49] and its partners. The nanomagnetic antennas showed 80 % reduction in size compared to traditional polymer substrate antennas.

5 Summary

Passive components for power and RF functions have been limiting the performance and miniaturization of electronic and bioelectronic systems. The inferior properties with these materials limit the component miniaturization, and hence,

these components are not integrated into active silicon CMOS devices or in packages. They are currently assembled as milli- or microscale components on the packages and boards.

Among the passives, magnetic components such as inductors and antennas have remained as the biggest bottleneck because of the limitations of traditional magnetic materials such as ferrites and microscale metal composites. Nanomaterials are emerging to address the fundamental limitations of today's magnetic materials. By designing the magnetic structures at nanoscale, simultaneous high-frequency permeability with low losses and power handling can be achieved. These nanomagnetic materials can thus transform today's bulky discrete magnetic components to integrated planar thin-film structures, resulting in simultaneous size reduction and performance enhancements. Similarly, nanoscale dielectrics and energy storage devices such as capacitors also increase the volumetric density with electrode surface area, high permittivity, high frequency, and thermal stability.

The superior properties of nanomaterials and their processability as thin-film 3D IPDs enable revolutionary advances for several power and RF applications such as high-density capacitors, inductors, filters, resonators, matching networks antennas, and EMI isolation structures.

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